

InCyte allows design teams, system architects and managers to visualize tradeoffs at the architectural stage of the IC design flow. It brings IP and manufacturing data to bear on the earliest stage of a chip plan, enabling better decisions regarding chip architecture, manufacturing technology options, and IP selection and integration. InCyte estimations take only seconds, and results typically correlate to within 98% of final silicon.

InCyte provides accurate estimation of the following key metrics.

- **Die area** Total die size and bounding, factoring in specified IP and design components.
- **Power** Dynamic power consumption computed factoring in frequency, switching activities, gate and IP data.
- **Leakage** Static power consumption computed by core, I/O, hierarchical block, as well as each IP macro.
- **Yield** Based upon industry or user-defined logic and memory defect density data
- **Cost** Calculated utilizing wafer pricing, yield, test & assembly, package, and non-recurring engineering (NRE) cost data.

To begin using InCyte, users enter a high-level design specification including gate count, clock speeds, I/O, and memory configurations. They select IP to be considered either by importing IP Lists they have built at ChipEstimate.com, or by choosing IP from the tool's customizable integrated IP catalog. InCyte then produces a comprehensive and accurate technical and economic chip.

InCyte is used to evaluate, explore and quantify IP and process technologies, and to achieve the optimal balance of chip functionality, performance and cost. Estimates are based on actual foundry, ASIC and IP vendor technology data models—the same design kit data used by chip implementation tools. For a comprehensive list of supported foundries and IP vendors, please visit www.ChipEstimate.com.

Results typically correlate to within 98% of silicon. Users can perform a rapid what-if analysis to compare their design across technology nodes, processes, IP options, and varying chip specifications.

InCyte's analysis of production chip cost uses economic data gathered from across the semiconductor design chain to provide a comprehensive and accurate economic analysis. The tool recommends a package based on technical estimation results, and then provides volume-based package pricing. Wafer pricing and defect density data enable systematic yield analysis and calculation of 'good die' cost. The analysis of design components provides an estimate of test and assembly costs, and NRE cost data provides process-specific mask cost estimations. InCyte's economic models are customizable, allowing users to override assumptions and tailor estimations to their needs. The result is a complete and customized budgetary quote.

InCyte can forecast chip cost over time, taking into account decreasing wafer costs, improving defect densities and other parameters. Return on investment analysis enables users to understand over what timeframe and volume NRE costs will be amortized, and when profitability on a design can be achieved.

Comprehensive datasheets and reports, including charts and tables describing die area usage, chip bounding, dynamic and static power consumption, yield, and production chip cost can be output. An early floorplan visualization and budgetary quotes can also be generated. All technical and economic results can be exported in a variety of formats. Design data may be exported in industry standard Verilog and LEF/DEF formats linking InCyte results directly into the chip implementation flow.

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InCyte Chip Estimation Products

InCyte Lite

InCyte Lite is the free, entry-level system for preliminary project feasibility analysis. Thousands of chip planners use InCyte Lite to compare different IP combinations and assess the impact of new process nodes and IP on new and existing designs. Estimates—based on industry average IP library and process models—provide an early estimate of die size, power and leakage. Download InCyte Lite at ChipEstimate.com.

InCyte

InCyte is used to establish and refine chip specifications, manage die and packaged chip costs, and aid in the exploration of various IP and foundry options. More information about InCyte can be found on the front of this datasheet. InCyte may be purchased and downloaded at ChipEstimate.com.

InCyte Enterprise

InCyte Enterprise is a customizable chip estimation system used by corporations to refine chip specifications and generate accurate IC quotations. The system accepts custom IP and process data, and models are tunable for increased accuracy. This client-server system delivers a local, dedicated chip estimation environment linked into internal databases and tightly integrated into chip implementation flows.

See reverse for product specifications.



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InCyte Chip Estimation Products			
	InCyte Lite	InCyte	InCyte Enterprise
Estimate			
Die size	■	■	■
Power consumption	■	■	■
Leakage	■	■	■
Yield		■	■
Die cost		■	■
Package recommendations		■	■
Production chip cost		■	■
Estimate with			
IP			
ChipEstimate.com IP catalog	■	■	■
Industry average IP libraries	■	■	■
Custom IP macros	■	■	■
Custom IP libraries			■
Foundries			
Industry average process data	■	■	■
Actual foundry process data		■	■
Custom process nodes			■
Tunable process models			■
Tunable economic models			■
Outputs			
Datasheet output	■	■	■
Charts and graphs	■	■	■
Side by side comparisons	■	■	■
Budgetary quote / cost breakdown		■	■
IC package recommendations		■	■
Floorplan export		■	■
Verilog export		■	■

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