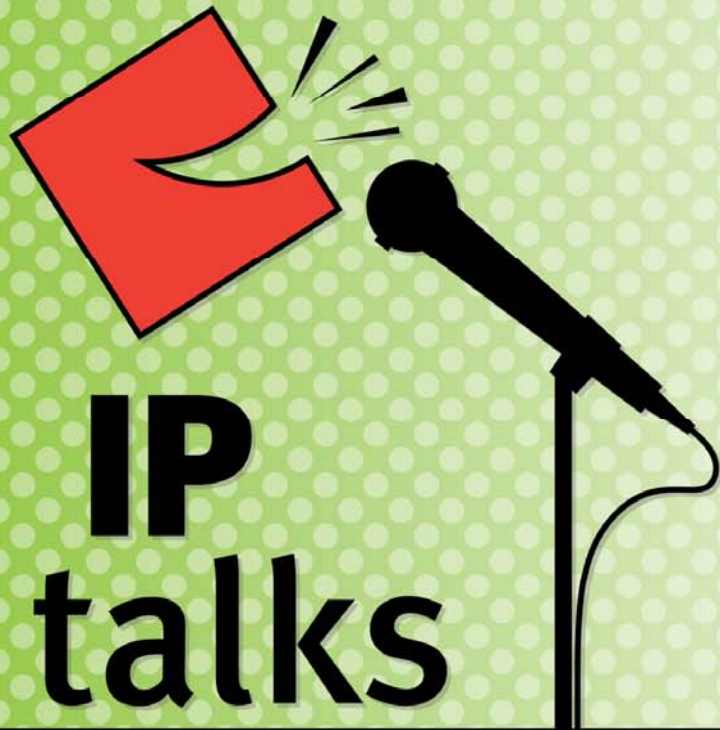




Colin Holehouse

*Active Power
Management*



Overview of ARC International



Company Highlights:

- The leading provider of configurable subsystems & cores for SoC design
- Holder of fundamental patents on configurability
- 140 customers worldwide
- Fastest unit growth of any Star IP company*

Future of SoC Design:

- Low power SoCs offering integrated video & audio functionality

Customer Commitment:

- Provide customers with a competitive advantage through low power configurable subsystems and cores that create differentiated, next-generation chips

**IP
talks**

* Semico Research, 2006

ChipEstimate™

Configurability for Different Markets



Wired & Wireless Networking



Consumer/Multimedia



Storage



- Configuration of the design for each target application means
 - Minimum design size, no silicon wastage
 - Lowest power design, no inactive functional blocks
- Extendibility means
 - Addition of specialized functions
 - Opportunities for further product differentiation



Power Management Techniques



Inactive Mode

- If the core is on “standby” for very long periods, then this may be the largest energy consumer
 - Techniques may have a high latency on being able to restart operation
1. Gate the clocks at the highest possible level
 2. Power down the core of the design

Active Mode

- Whilst the core is operating the highest power is consumed.
 - Techniques must have no impact on achieving the intended result
 - May impact the elapsed time of achieving the intended result
1. Gate the clocks for a function when it is not in use
 2. Reduce the voltage and frequency for non-compute intensive operations

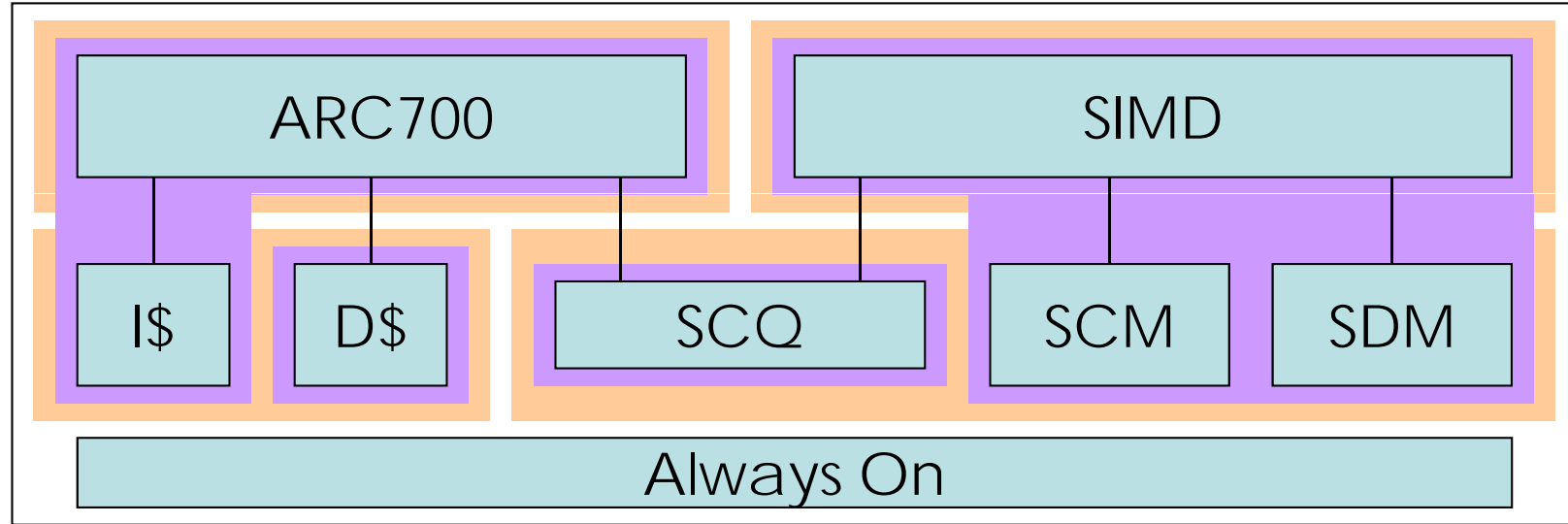


Power Intent



Legend

- Functional Blocks
- Clock Gating Domains
- Power Domains



Name	Voltage
HIGH	1.2V
NOM	1.0V
LOW	0.8V

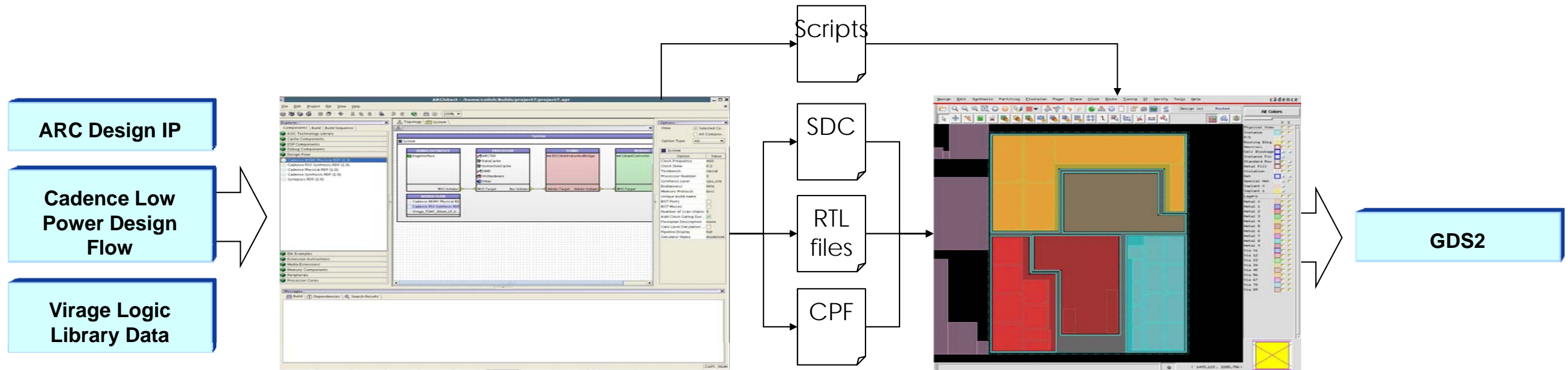
Perf. Mode	Switched Power Domain	
	RAM	CORE
C0	HIGH	HIGH
C1	HIGH	NOM
C2	NOM	LOW
C3	LOW	LOW

Mode	Switched Power Domain							
	CACHE/SIMD_RAM*				CORE/SIMD*			
	C0	C1	C2	C3	C0	C1	C2	C3
PD0	H	H	N	L	H	N	L	L
PD1	H	H	N	L	H	N	L	L
PD2	L	L	L	L	0	0	0	0
PD3	0	0	0	0	0	0	0	0

*SIMD may be powered down independently



Reference Design Flow



- ARChitect configures the design together with the design flow and library data
- The flow is being developed in partnership with Cadence Design Systems.
- Library data, including specialist low power cells, have been supplied by Virage Logic.
- CPF describes the power intent and ensures consistent implementation across all tools in the design flow.



Thank you!



- Please stay and talk with Colin
- Explore ARC IP at ChipEstimate.com
- Use ARC IP to Plan a Chip at DAC (get a DAC Trip Report!)

