



**Chad Spackman**  
*Founder*



# Overview



- Hardware Acceleration for Data Networking and Storage Applications
  - New tools to overcome limits of RTL hardware design for high performance, large scale design
    - C2R Compiler
  - Development Framework for efficient delivery of complex components
    - CebaIP Platform
  - 3<sup>rd</sup> Party Provider of Networking and related IP Cores

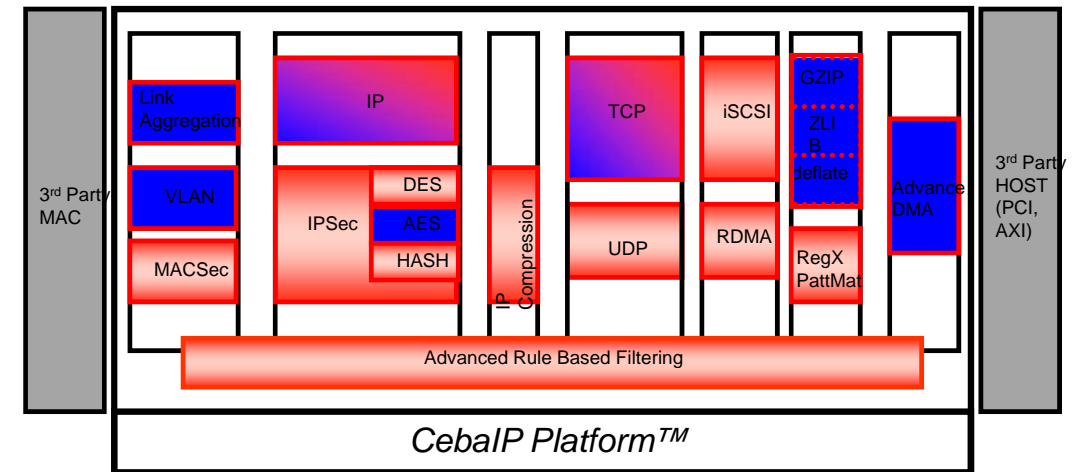


# CebaIP Products



- CebaIP Platform

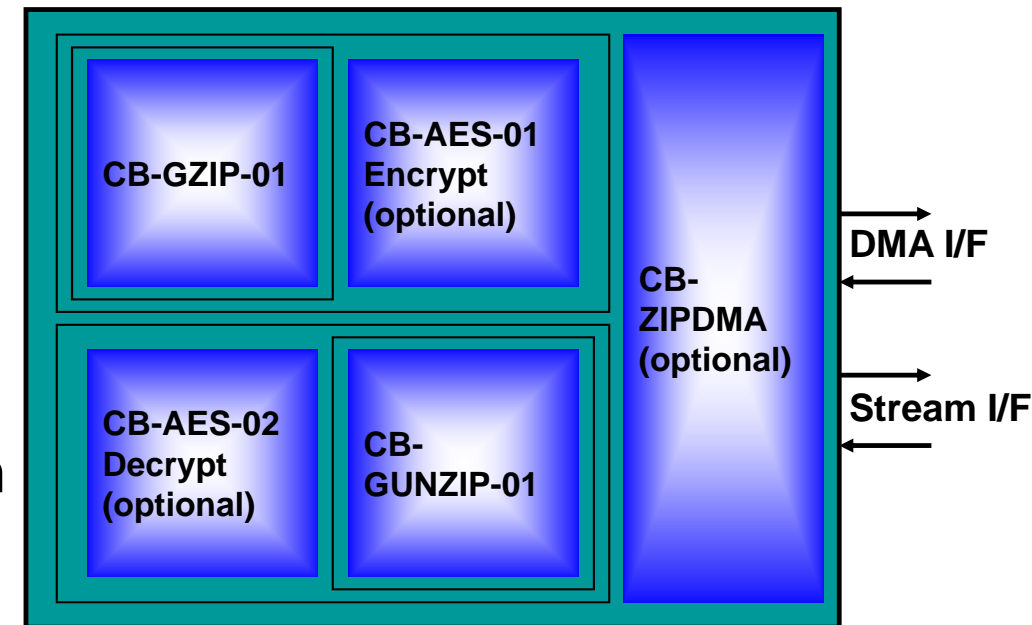
- Framework for developing data and storage networking IP cores
  - C2R Compiler™ C-to-RTL technology
- Modular approach to offering end-to-end solutions
  - Flexible customization
  - Predictable design results
- Supports ASIC and FPGA implementations



# CebaIP Products



- CebaIP GZIP Family of IP Cores
  - Lossless Data Compression/Decompression
    - RFC1951 with RFC1950, RFC1952 compliance
    - Optional AES encryption with IEEE 1619 Compatibility
    - Optional Advanced Descriptor-based DMA engine
    - Optional Dynamic Huffman Table support
  - 1Gb/s to 10Gb/s Throughput
  - 2.5:1 to 3.5:1 and as high as 10:1 Compression



# CebaIP GZIP Applications



- Storage Control Systems
  - Virtual Tape Libraries (VTL)
  - Disk, Tape and Flash Storage Media
  - Embedded Storage Processors
- Data Networking Systems
  - Web Servers and Web Appliances
  - Router and Content Switches
  - Embedded CPU's



# Thank you!



- Please stay and talk with Chad
- Explore CebaTech IP at [ChipEstimate.com](http://ChipEstimate.com)
- Use CebaTech IP to Plan a Chip at DAC (get a DAC Trip Report!)

