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PLDA



- **Mission**
 - Provide PCI-related IP to ASIC/FPGA designers
- **Expertise in PCIe, PCIX and PCI technologies**
 - #1 PCI IP vendor worldwide, ([Gartner Dataquest 2005/2006](#))
 - 2000+ licensees worldwide
- **PLDA as PCIe IP vendor**
 - #1 Worldwide for FPGA and ASIC PCIe IP Market
 - PCIe IP on PCI-SIG Integrators List
 - 600+ PCI Express licenses worldwide
 - Customers include: Cisco, Agilent, Sony, HP, Hitachi...
 - High quality Support and Design Services available worldwide
 - US (San Jose, Austin) and European offices
 - Distribution network Worldwide



PCI Express IP

- **PCI Express 'Rich' Core**
 - ASIC and Structured ASIC Core
 - Supported on high-end FPGA
- **PCI Express 'Lite' Core**
 - FPGA optimized Core
 - Supported on low-cost and high-end FPGA
- **Bridge IP Core**
 - PCI/PCI-X to PCI Express reverse bridge
 - PCI Express switch reference design
 - AHB to PCI Express bridge
 - AXI to PCI Express bridge



PCI Express Core

Technical Facts

- **Soft Core**
 - Clear-text VHDL and Verilog RTL source code
- **Compliant with PCI Express rev.1.1 Specification**
 - Extensive support for optional features (multifunction, MSI-X, AER, ECRC, Hot Plug, ...)
- **x1, x4 and x8 available**
 - 64-bit data path
 - PIPE compliant 125MHz (x1, x4) and 250MHz (x1, x4, x8)
- **All three digital layers implemented**
 - MAC, Data Link and Transaction layer
 - PCS layer available for non-PIPE PHYs
- **Application layer interface**
 - Per-VC Receive/Transmit (Tx/Rx)
 - Optional Master/Slave with multi-DMA capability (EZ)
 - Single VC endpoint only
- **Supported configurations**
 - Native/Legacy Endpoint
 - Root Port
 - Dual-mode Root Port/Endpoint (shared silicon)
 - Switch Upstream/Downstream
 - Forward/Reverse Bridge



PCI Express Rich Core PLDA Specific Features

- Extensive debug capabilities
 - 32-bit input port allows for error injection, scrambling control, compliance control, and more...
 - 512-bit output port allows for status and monitoring through error reporting, FSM state probing, and more...
- Flexible receive buffer modeling
 - Per-VC dedicated buffer or common buffer
 - Support for ECC protection
- Physical Coding Sublayer (PCS) available for custom PHY interfacing
- Transaction layer bypass for custom designs



Thank you!



- Please stay and talk with Owen
- Explore PLDA IP at ChipEstimate.com
- Use PLDA IP to Plan a Chip at DAC (get a DAC Trip Report!)

