



cādence™

Cadence Verification IP

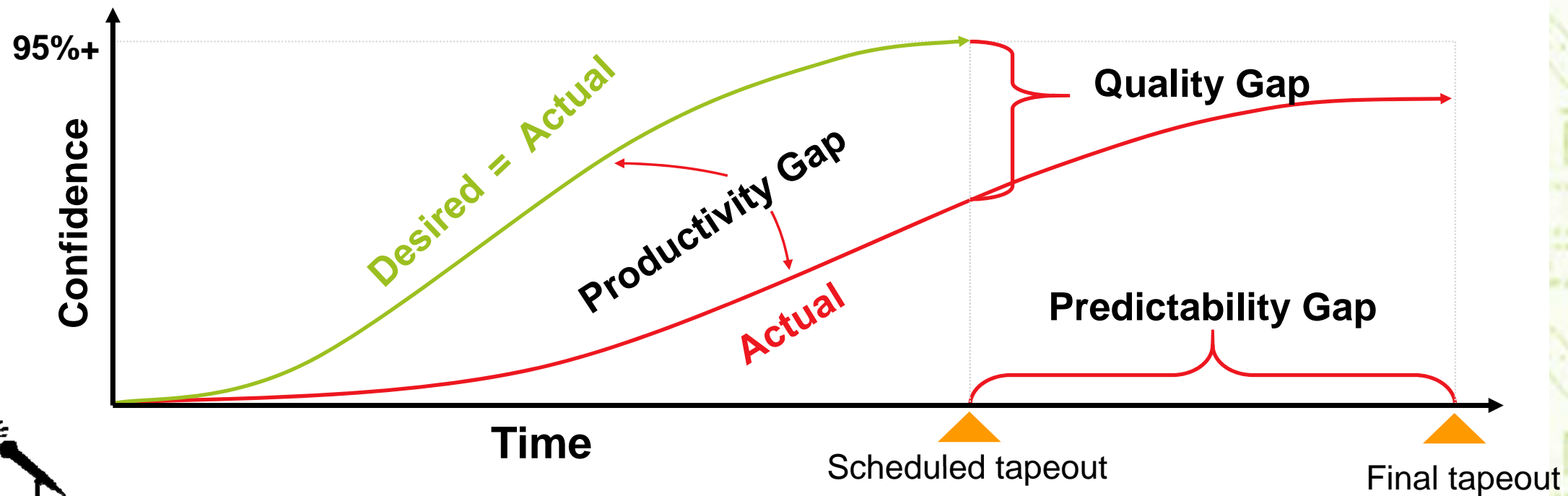
Dave Tokic

Director, Product Marketing

Customer Verification Goals

Need : Automated and pre-packaged solution for verification closure

- Predictability: Compliance management delivers verification closure metrics “out of the box”
- Productivity: Accelerate environment development and reuse by 2-10x
- Quality: Leverage mature, protocol complete, and automated compliance to catch hard bugs



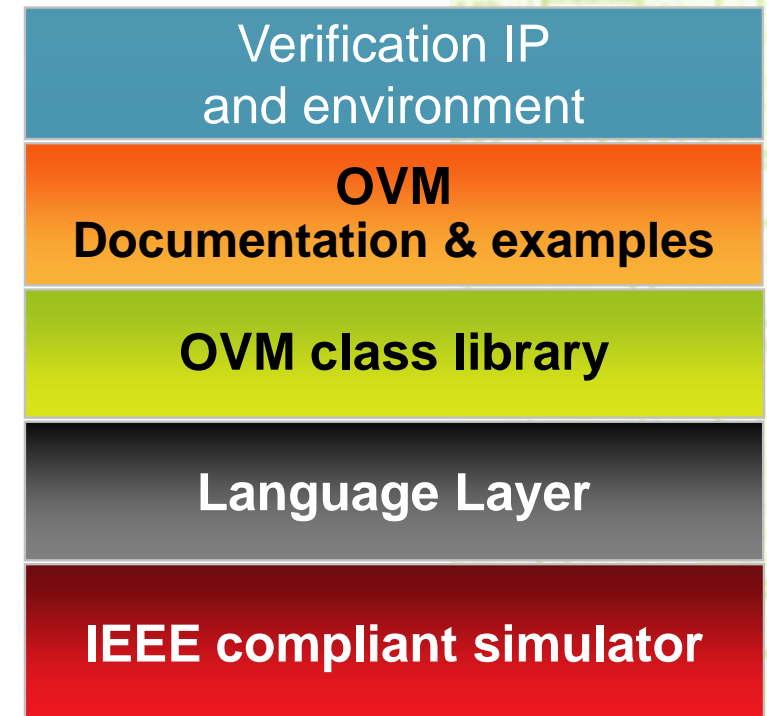
Delivering On Our Vision: The Open Verification Methodology (“OVM”)

- Open, interoperable, and proven verification re-use methodology
 - Runs on any IEEE 1800 compliant simulator
 - Open to all via the Apache open source license
- Jointly developed with contributions from Cadence’s Incisive® Plan-to-Closure URM module, and Mentor’s AVM
- Benefits
 - Enables interoperability and reuse across projects, and a whole industry VIP ecosystem
 - “Plug and Play” interoperability with *e*, SystemC, and non-OO, module-based SystemVerilog approaches
 - Interoperable and reusable with *e*RM compliant VIP
 - Scalable to system level
 - Maturity: Leverages the time-tested *e* Reuse Methodology

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<http://www.ovmworld.org>



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Mentor
Graphics®

ChipEstimate.com™



Cadence Verification IP

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Plan-to-Closure VIP pre-packages Metric-driven verification

Compliance Management System (CMS)

UVC

OVM Interface | eRM Interface

Advanced Testbench Core

Assertion Based VIP

Transaction Based Acceleration

Emulation SpeedBridge™

- Production proven in over 2,000 projects
- Supports full spectrum of verification needs
- Available for most demanded protocols

ARM
AHB

ARM
AXI

PCI
EXPRESS™

mipi™ *New!*
mobile industry
processor interface

Ethernet

USB
SuperSpeed
USB
On-The-Go

OCP
International Partners

SERIAL
ATA

PCI
CONFORMANCE

- Unique Compliance Management System (CMS) automates compliance verification
- Customer enablement and 3rd party ecosystem expands VIP portfolio



IP
Talks!



ChipEstimate.com™



Industry-leading VIP Ecosystem



 Supplied by Verification Alliance Partners
 Supplied by Cadence



PCI-X

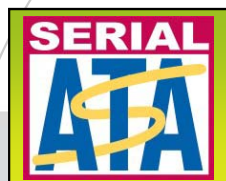
I²C

Bus and Interconnect

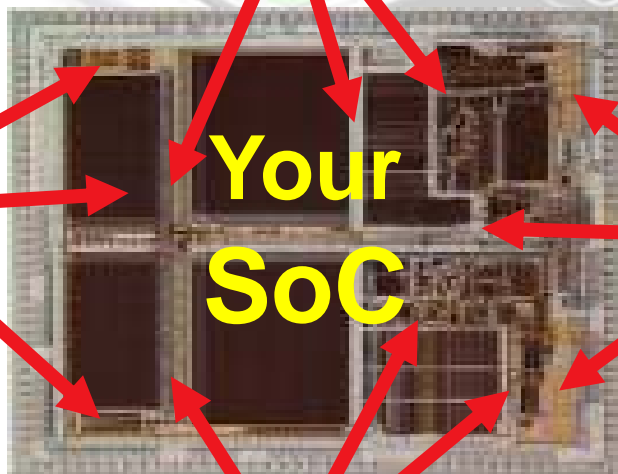
PCI

Ethernet

SONET



Compact Flash



Your SoC

IEEE1394



Fibrechannel

Storage

Serial Protocols



CE-ATA



SAS

SDIO

ATAPI

irDA

SPI-4

MPEG

Communications

AVC

Automotive CAN LIN

Wireless USB

DFT Verification



IEEE P1500 Embedded Core Test

JTAG

UART



ChipEstimate.com



Announcing Cadence OVM-Compliant VIP



Growing the OVM Ecosystem

MARKETWIRE - JUNE 9, 2008

Cadence Delivers OVM-Compliant Verification IP

Cadence Verification IP Enables Open Verification Methodology (OVM) Users to Automate Protocol Verification and Compliance to Meet Schedule Demands

SAN JOSE, Calif., June 9, 2008 -- Cadence Design Systems, Inc. (NASDAQ: CDNS), a global electronic design innovation, today announced the availability of two new testbench verification IP (VIP) products that are compliant with the Open Verification Methodology (OVM). These enhancements enable the rapidly growing community of OVM users to easily access Cadence® metric-driven verification solutions and to predictably achieve high-quality verification closure. The AMBA® 3 AXI™ and AMBA AHB™ VIP, having been proven on hundreds of designs, are now available as multi-language Universal Verification Components (UVC) and are the first to provide OVM support within the Cadence VIP portfolio. OVM support will be added to the remaining protocols in the VIP portfolio in the second half of 2008.

The first two OVM-compliant advanced testbench VIP in Cadence portfolio
AMBA 3 AXI and AMBA AHB

Seamless integration into OVM SystemVerilog environments

Metric-driven verification
Unique CMS & multi-language support



Compliance Management System (CMS)

Cadence
Only!

cadence™

Automatically Achieves High Functional Coverage

- Included with UVCs to automate compliance verification and reporting
- Developed with leading protocol experts (e.g., ARM, AMD)
- Applicable to both Design IP and SOC developers
- Correlates coverage directly to protocol specifications

Executable representation
of verification objectives

Compliance
Management System

Compliance
User Interface

Compliance
Coverage
Model

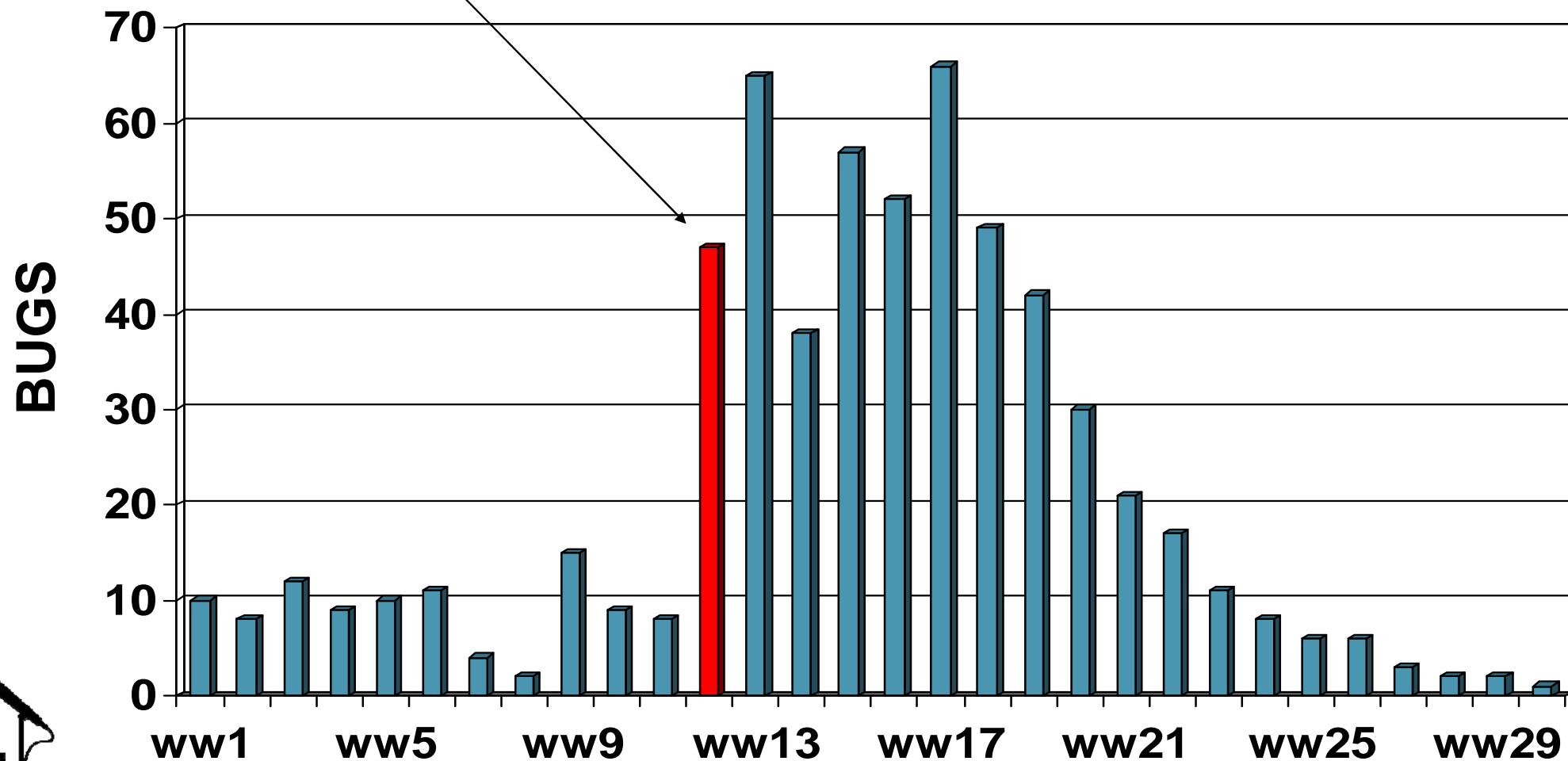
Compliance
Checks and
Metrics

Library of constrained
random tests to fill
coverage map



Metric Driven Verification with CMS: Increasing Bug Discovery Rate

Large-Scale Coverage Deployed on Existing Customer Project



CMS Success Story: ClearSpeed

Metric-Driven Verification Improves Quality, Productivity and Predictability

- Found DUT bugs faster: 4 in first day!
- Dramatically increased PCI Express compliance coverage
 - Taped out at 96% coverage
 - Significantly reduced respin risk
- Major improvement in project management and resource assignment using coverage, bugs, and test failure metrics
- Much improved team communications

“With CMS our team leaders now confidently report on verification status in all functional areas including coverage, bug rates and test failures.”

Mike Bartley
Test and Verification Manager

For details see:

http://www.cadence.com/company/newsroom/press_releases/pr.aspx?xml=040907_ClearSpeed





Summary

cadence™

- Proven, industry-leading VIP spanning the verification process
- OVM support providing multi-language reusability
- Unique metric-driven compliance management system



Thank you

- Explore Cadence Verification IP at ChipEstimate.com
- Use Cadence's leading Verification IP to verify your next chip!
- Please stay and talk with Dave Tokic

