



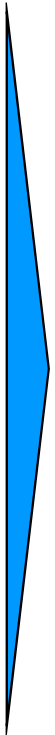
Chad Spackman
CTO, Founder

Overview



- **Cebatech develops and markets ESL tools for advanced ASIC, FPGA and SoC design, and uses these tools to create and license high-value IP cores – CebaIP™ Products**

Cebatech Design Flow

- True ANSI C to RTL compiler
 - Intuitive mapping of C constructs to Hardware
 - Complete Language support
 - Pointers
 - Pointer Mathematics
 - Function Calls w/ Arguments
 - Global Variable
 - System wide multi-writer
 - All C complex data types
 - Variable Mapping to System Memory
 - Looping
 - Loop unrolling
 - Hardware Pipelining
 - Control and/or datapath dominated design
 - Standard Language that facilitates the highest level of hardware abstraction
 - Verification in native software environment
 - Environment that facilitates SW/HW co-design and system architectural exploration
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- Non-standard specifications: Domains that have moving specifications can hugely benefit from this ESL flow
 - For e.g. in case of Deduplication:
 - No Standards
 - Architecture in flux
 - SW/HW quotients under exploration
 - Control & Datapath components are to be finalized
 - Flexible Design Approach: C2R allows software under development to be explored in hardware
 - Time to Market: C2R allows software/hardware interfaces & drivers to be concurrently developed with hardware, which reduces time to market
 - Design Cost: Reduced resource requirements, shortened design cycles, and minimum re-spins.
 - Rapid Reconfiguration: Future designs can rapidly adapt to changing market requirements



CebaIP Products



- Hardware Acceleration for Data Networking and Storage Applications
 - GZIP/Deflate – Lossless Data Compression
 - LZRW3 – Lossless Data Compression

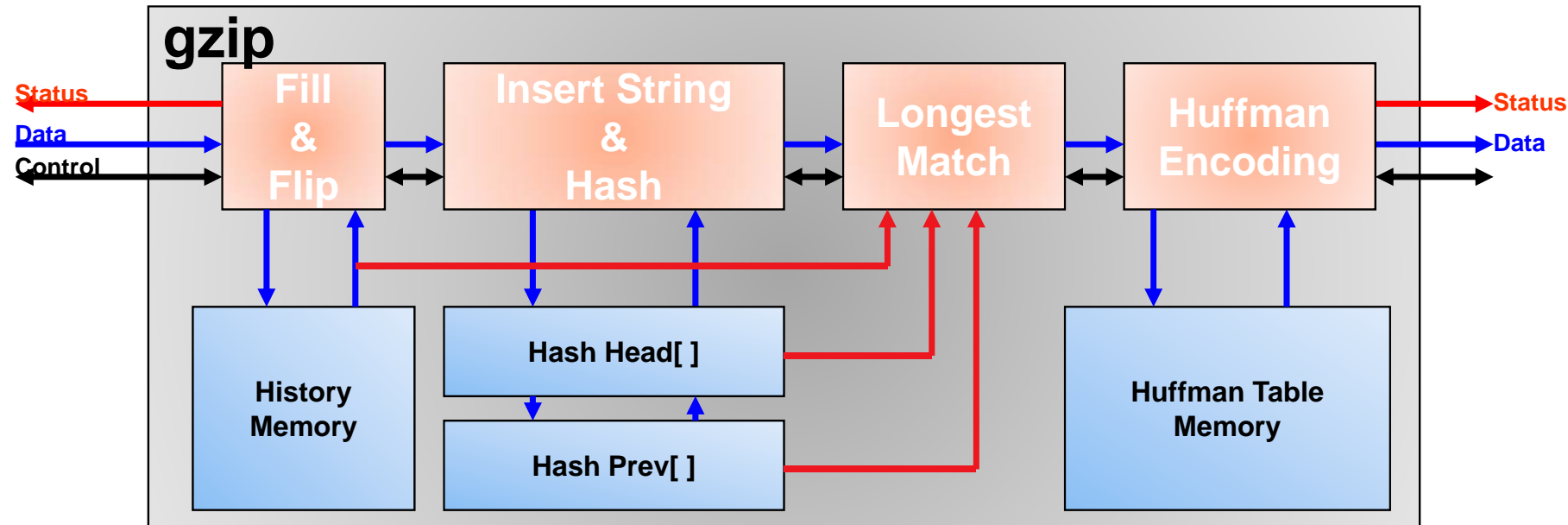
CebaTech's ESL approach enables precise modeling/creation of software algorithms, conversion of proven software code to robust hardware, and rapid customization to application requirements



CebaIP GZIP Family of IP Cores



- RFC1951 with RFC1950, RFC1952 compliance
- Optional Dynamic Huffman Table support
- 1Gb/s to 8 Gb/s Throughput
- 2.5:1 to 3.5:1 and as high as 10:1 Compression

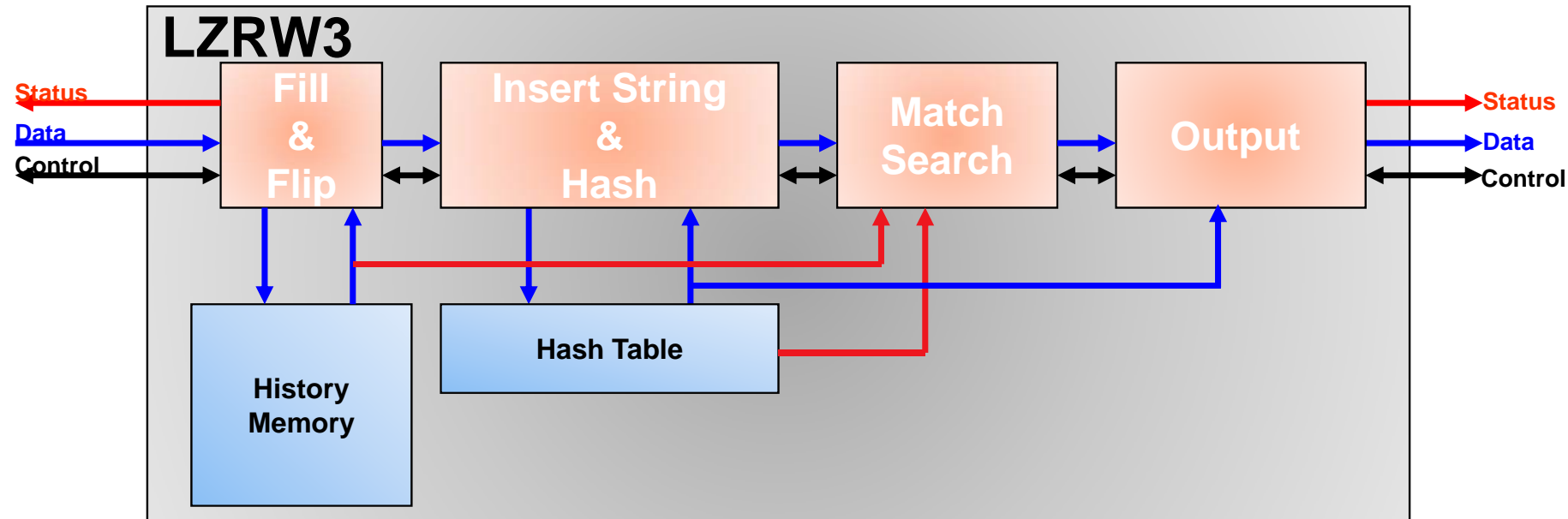


CebaTech GZIP Compression for bundling with Storage Management applications –
e.g., encryption, de-duplication



CebaIP LZRW3 IP Cores

- Fully conformant with Ross Williams software algorithm
- Capable of data throughputs in excess of 2Gbps
- Compression ratios of 2:1 and greater



CebaTech LZRW3 Compression for bundling with Storage Management applications –
e.g., encryption, de-duplication

Thank you



- Explore CebaTech IP at ChipEstimate.com
- Use CebaTech IP to plan your next chip!
- Please stay and talk with Chad Spackman

