



denali

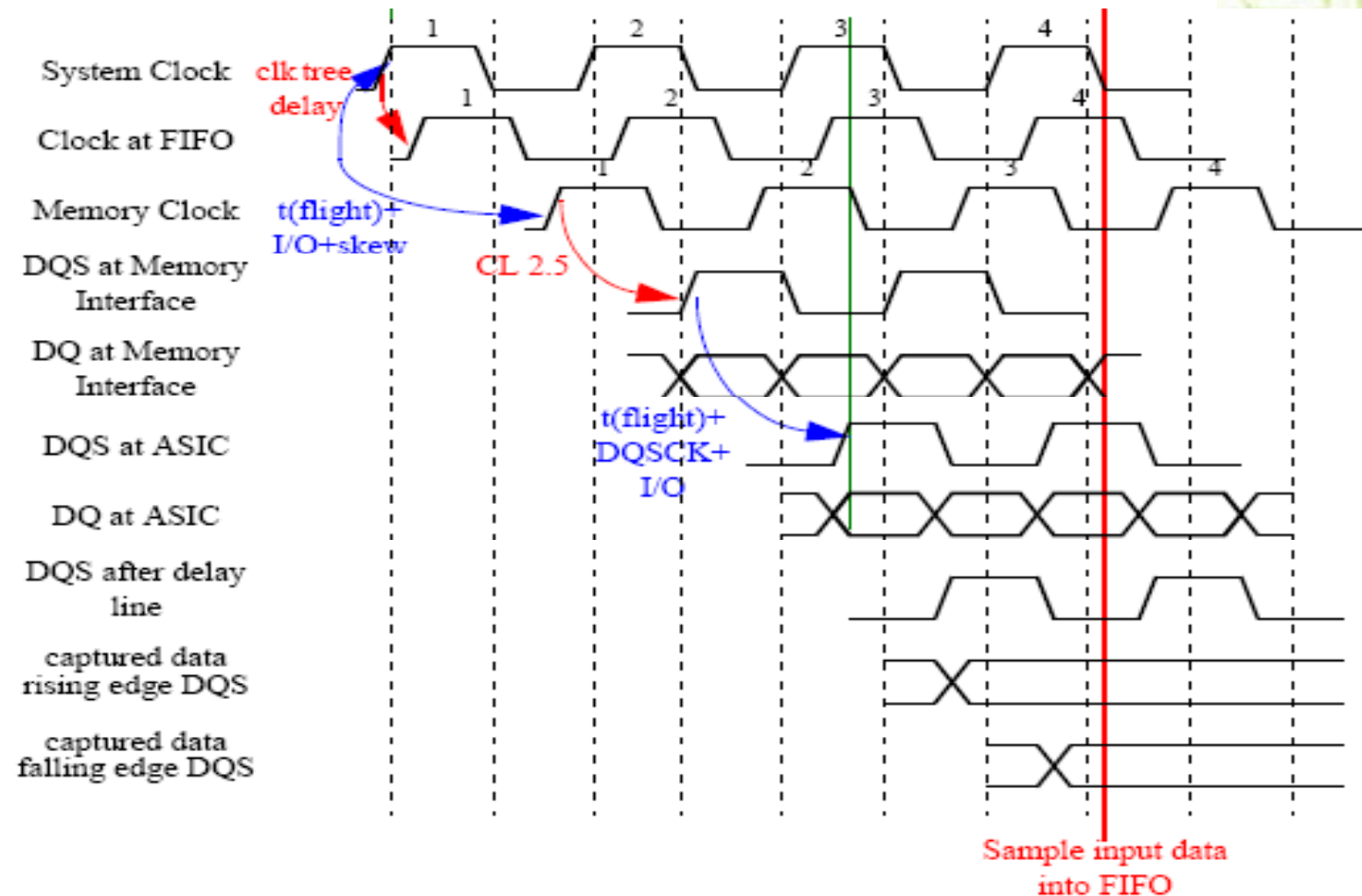
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DDR Memory: a Big, Common Problem

- DDR memory is now on the majority of SoC's
- DDR PHY creation and timing closure now often paces the chip schedule
 - Hundreds of highly skilled engineering hours
 - Large toolset needed
- It's much more than connecting a DLL and IO pads!!
- PHY speeds are rapidly increasing, and timing closure is getting geometrically harder

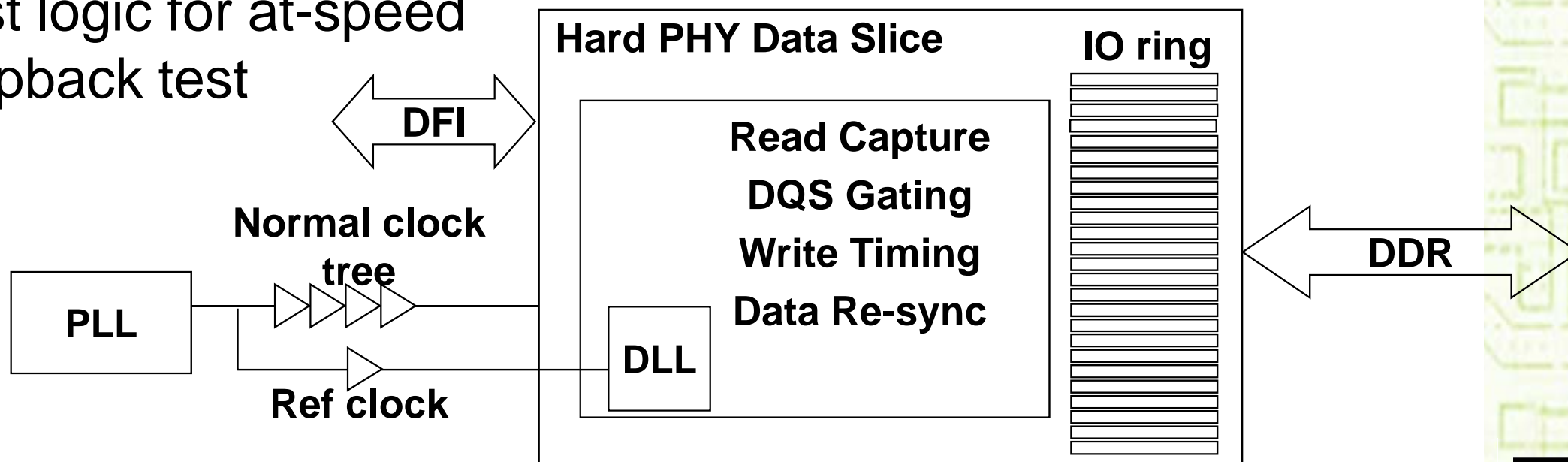
Why is the PHY difficult?

- Tight timing margins
- Wide busses, large skews, much SI noise
- Explaining how multiple clock domain timing and layout works to the EDA tools
- Controlling latency
- Proving that the PHY design will work

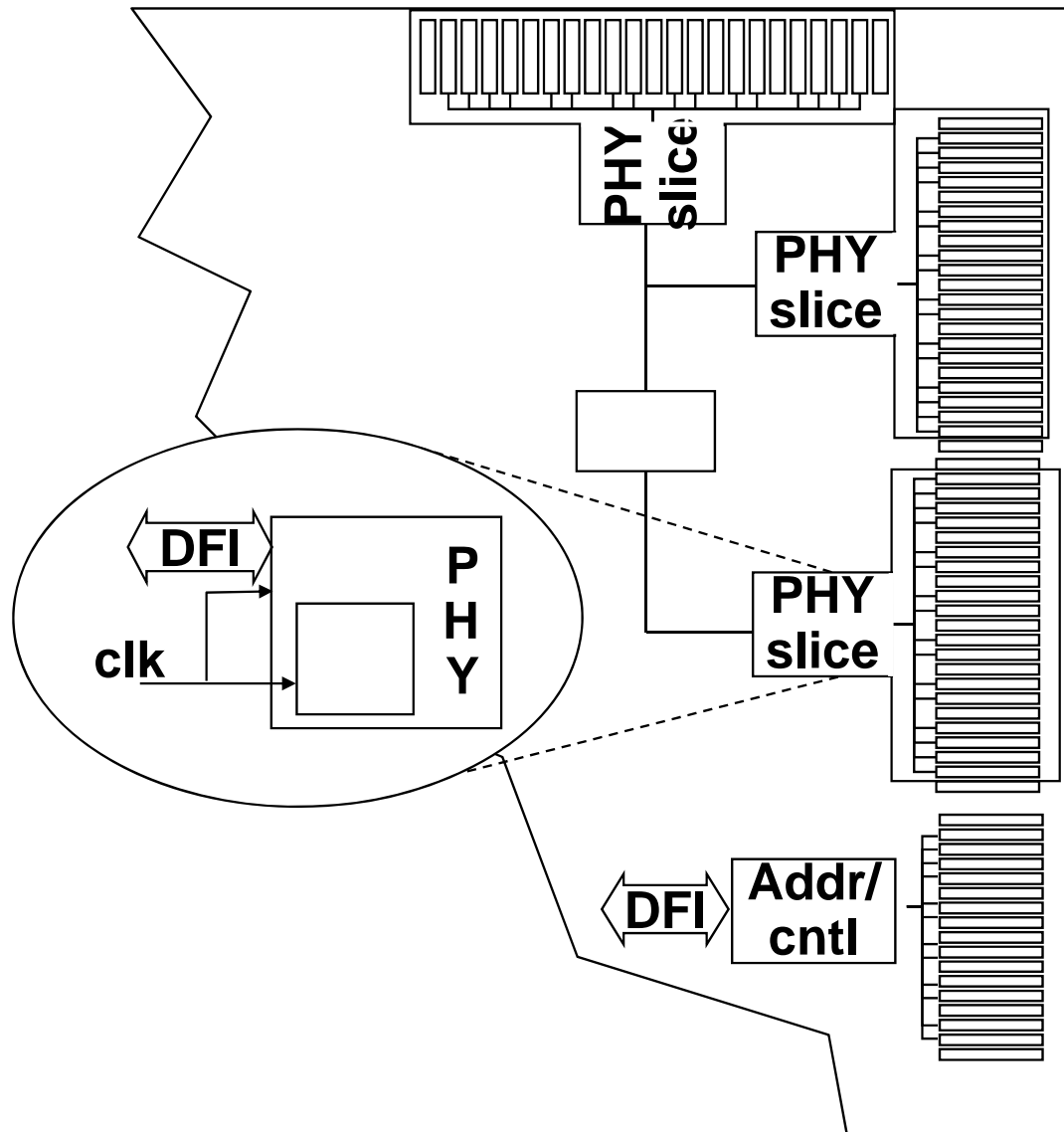


PHY Architectural Overview

- Separate PLL
 - Use for multiple slices
 - Can use for rest of chip
- Fully hardened 8-bit data slice
 - Highly reusable
 - Keep “on the shelf”
- Test logic for at-speed loopback test
- Clock reference
 - Minimally buffered PLL input to slice for source synchronous domain
 - Normal clock tree for DFI, flop-to-flop timing



PHY Physical Structure

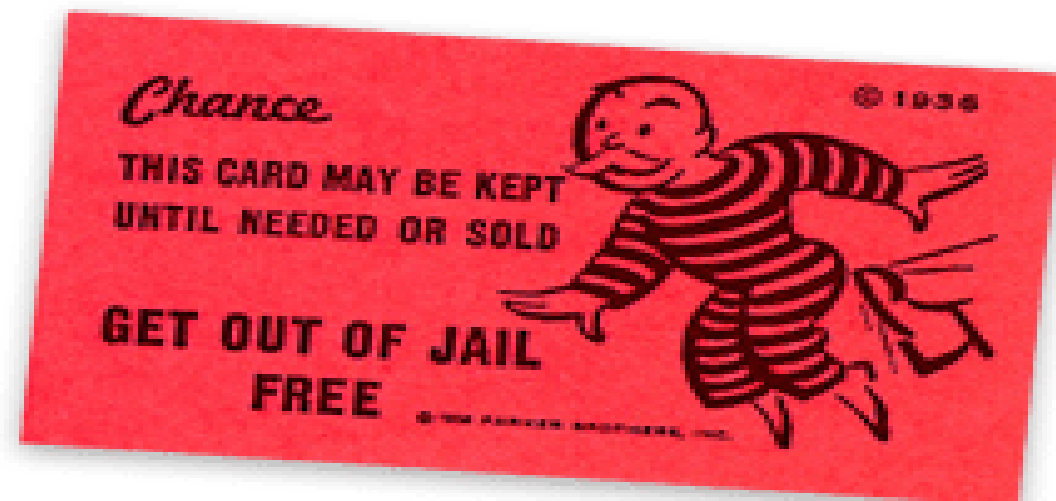


- Flexible structure
- Synthesized address and control
- Very adaptable to different floor plan needs
 - Chip size
 - Pad type, package type
 - Bus Width
 - Power/ground ratios
 - DLL does not require special power due to built-in isolation
 - ESD strategies

PHY Architectural Choices

- Overall Architecture
 - Designed for reuse
 - Proven in more than 50 customer designs
 - Denali's 3rd generation PHY
 - Highly flexible, highly tunable
 - 1X Clock, multiple DLLs

***Every tuning option is a
“Get out of Jail Free” card...***

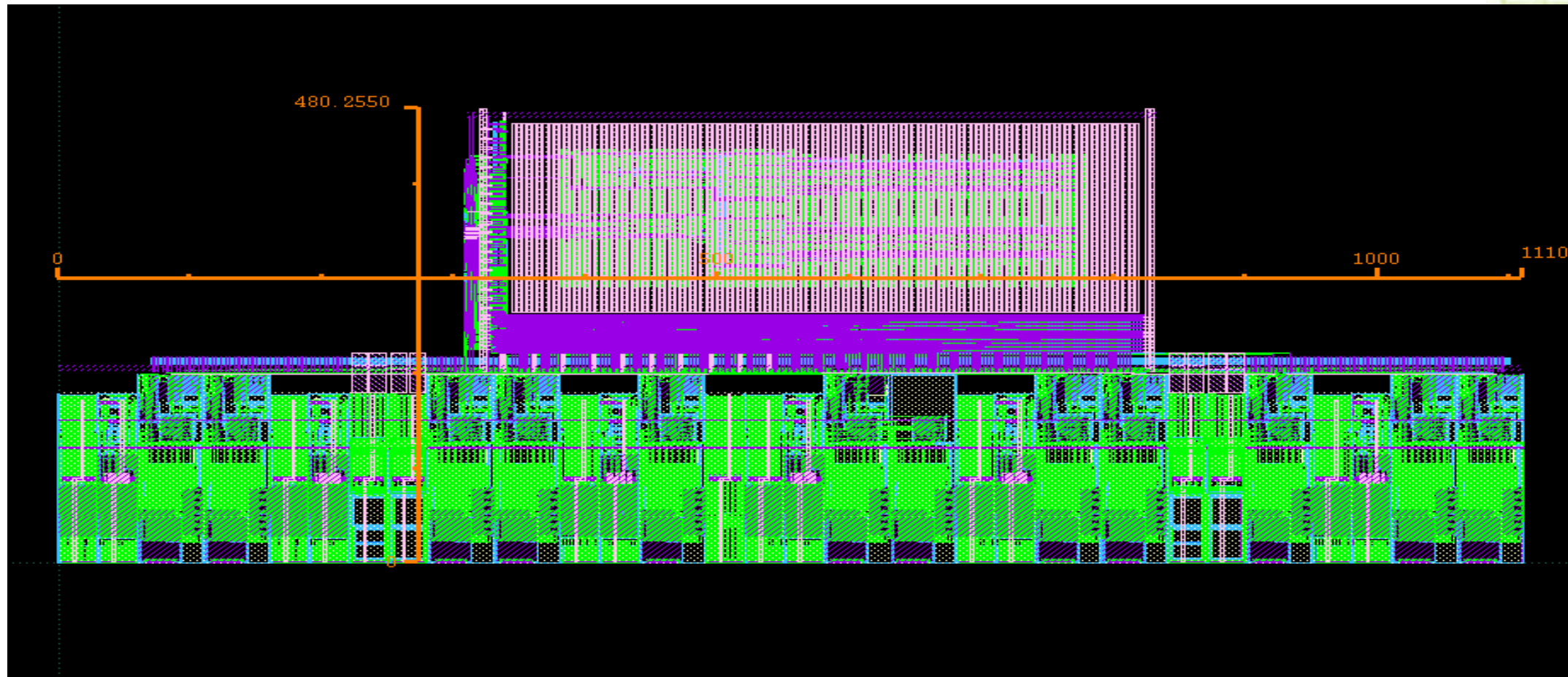


Key Points of the DDR PHY Solution

- Configurable
- Complete
 - Logical views: RTL/models for simulations and tuning
 - Physical views for floorplanning and implementation
 - Timing budget tools and verification suite
 - All scripts, constraints, .lib files and users manual
- Flexible
 - Integrate to different IO pads
 - Adaptable to different chips and processes
- Brings complete domain knowledge
- Built on proven, high quality technology platform
 - Built on Databahn configurable platform, which has produced 250+ designs, 100+ in silicon (**100% success**)

Denali PHY Physical Design Flow

- Completed Chartered 65G data slice with pads
- Denali Hard IP available now



Summary

- Denali PHY architecture is silicon proven in more than 50 Denali customer PHYs
- Denali team has extensive PHY hardening experience
- Denali's Hard PHY is built on best-in-class silicon-proven parts
- Denali can provide a complete, timing-closed GDSII Hard PHY with more flexibility and less risk than our competitors

Thank you



- Explore Denali's IP and Hard PHY at ChipEstimate.com
<http://chipestimate.com/vendorlist.php?v=261>
- Use Denali IP and Hard PHY in your next chip!
<http://denali.com/dram>
- Please stay and talk with Rayfes Mondal

