



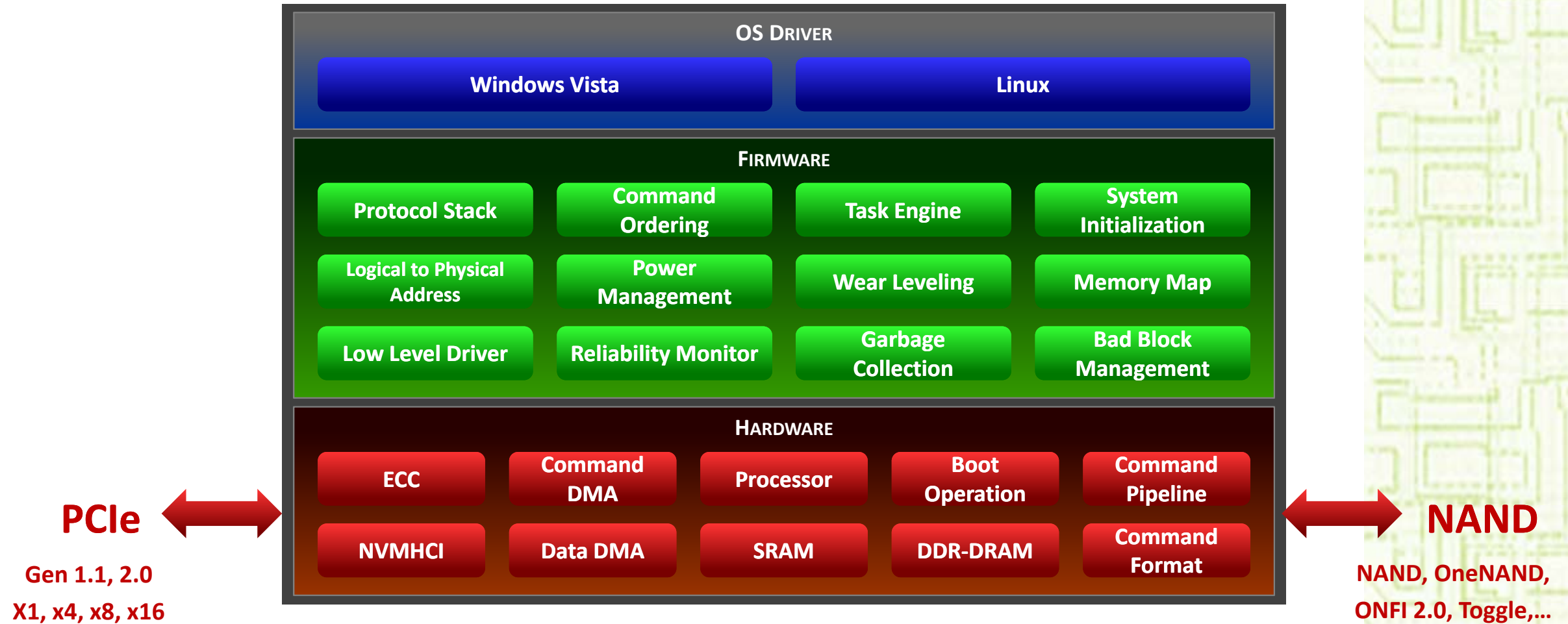
*denali*

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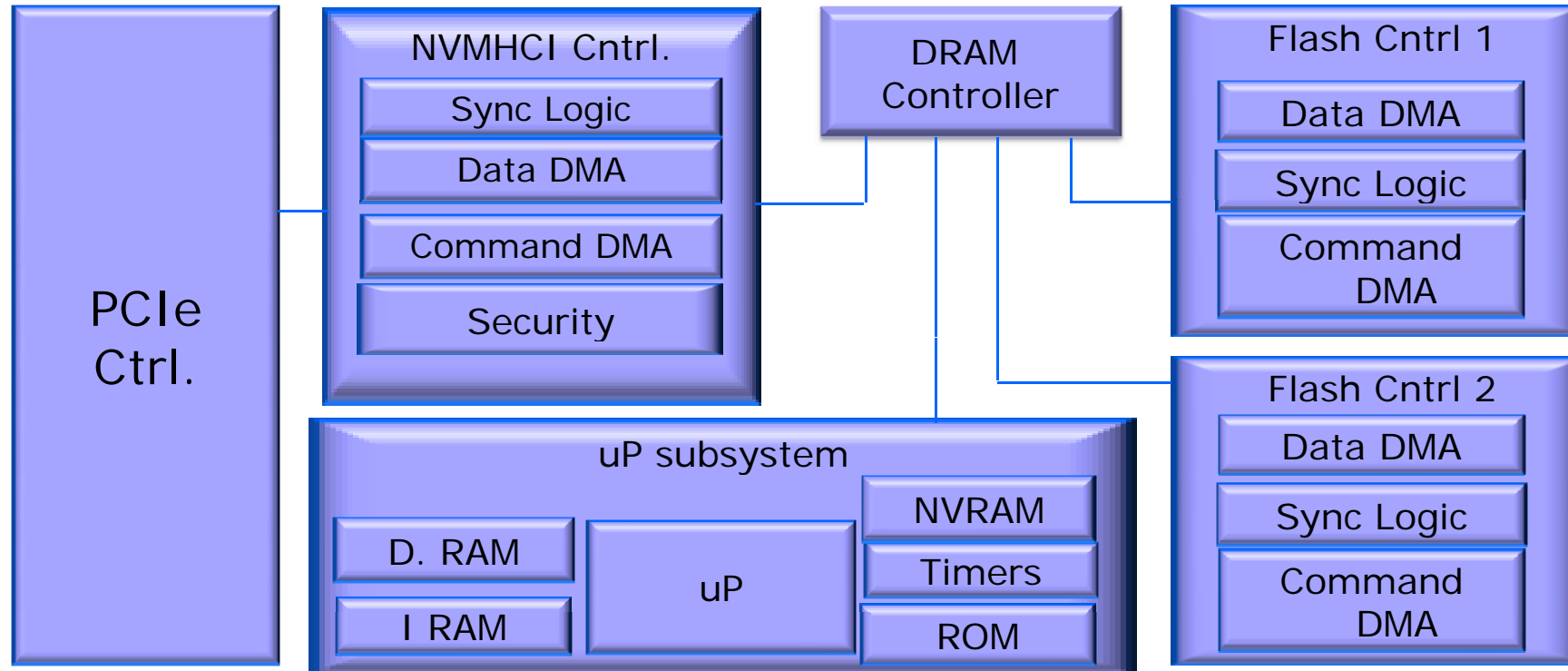
# Embedded Design Challenges

- Meet performance objectives
  - CPU performance
  - Cache sizing
  - Multi-bus masters (bus routing)
- Cost objectives
  - Architecture tradeoffs
  - Process
  - Packaging
  - Physical layer's
- Power management

# Denali PCIe-Flash Platform



# Top-Level Architecture



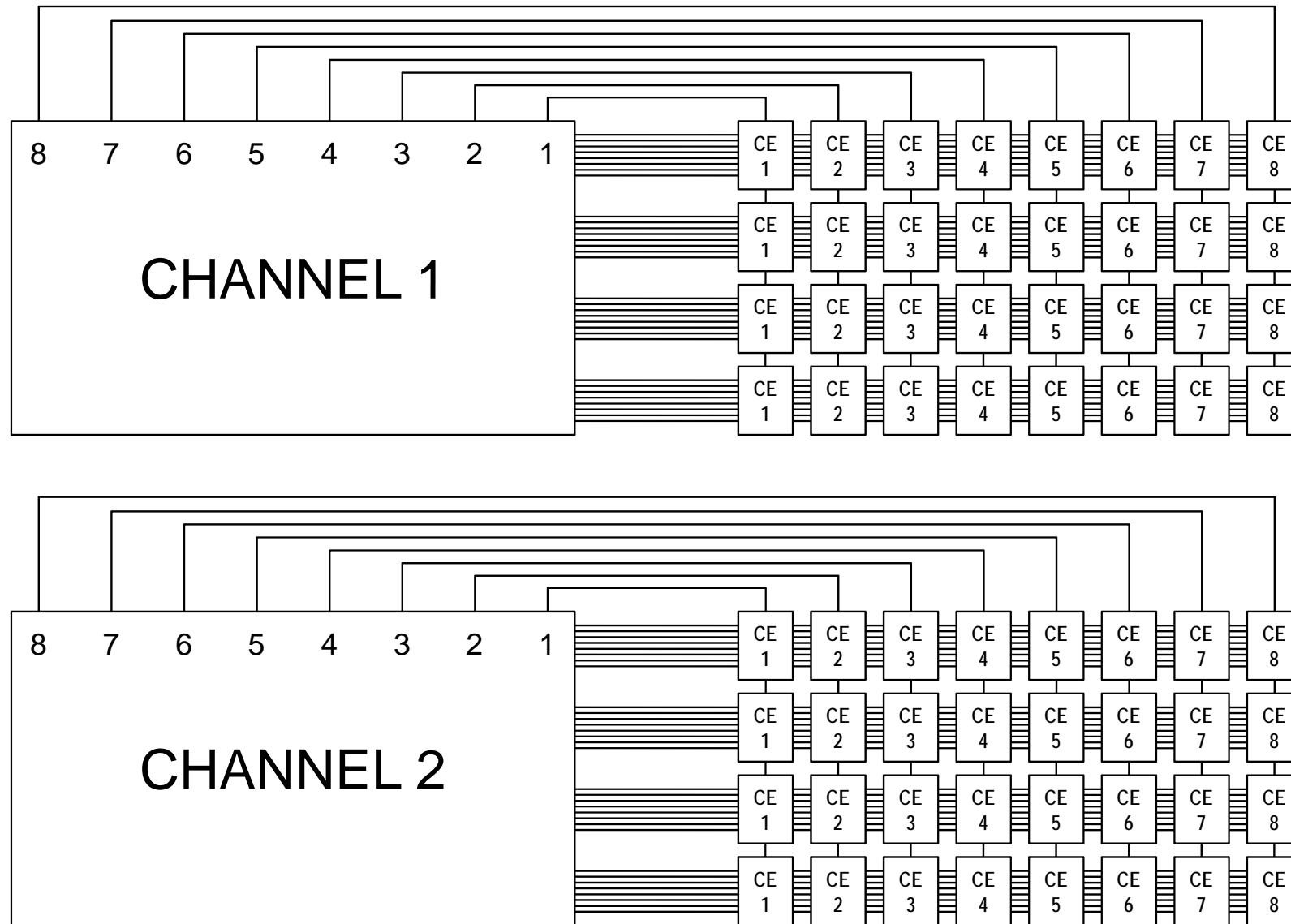
- Hardware accelerated architecture
- Multi-bus master
- Tightly coupled RAM blocks for block table
- Multi-thread LLD
- Large command queue to optimize throughput
- External DRAM for additional buffer
- DMA arbitration

# Denali Platform Flexibility

Design Elements	Base Design	Video Server Requirements
Flash Controller Cores	2	2
Chip Enables	8	16
Flash Controller Bus Width	32	64
ECC bits	8	8
Number of Command DMA's	3	5
Number of Data DMA's	2	2
PCIe Controller Lanes	1	8
NAND Device Type	Standard SLC	ONFI 2.0
External DRAM	Base Design	Video Server Requirements
Bus Width	32 bit	64 bit
DRAM Device Type	LP-DDR2	DDR2
Clock Rate	200MHz	200MHz
Firmware	Base Design	Video Server Requirements
Task Switching Engine	(std)	Modified
Flash Translation Layer	(std)	Modified
Low Level Driver	(std)	Modified
NVMHCI Software Stack	(std)	Modified

- RTL modifications: *Moderate*
- Firmware modifications: *Moderate/Significant*
- FPGA implementation: *Moderate/Significant*

# Memory Access



- 2 independent channels
- 8 chip enables
- Depth expansion 4 to 8 devices
- Addressing 128 to 256 GB per FPGA (package)
- All mounted on a custom DIMM

# Tradeoff in Design

- Critical features that are SW/FW enabled
- Additional overhead for multi use scenarios
- Maximize performance and upgradability
- Security
- Data integrity during power loss
- Multiple flash Interfaces
  - NAND
  - Toggle
  - ONFi 1/2

# Conclusion

- Flash is a market that requires the best performance, reliability and flexibility
- Smaller geometries are requiring more technology to be developed
- Multiple applications and bus traffic differ greatly between applications
- A tool to do architectural exploration is imperative to meet the market constraints in a timely manner
- Maximum HW flexibility permits designs to be SW/FW upgradeable to meet future flash requirements

# Thank you



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