



Ashraf Takla
President & CEO

Company Profile

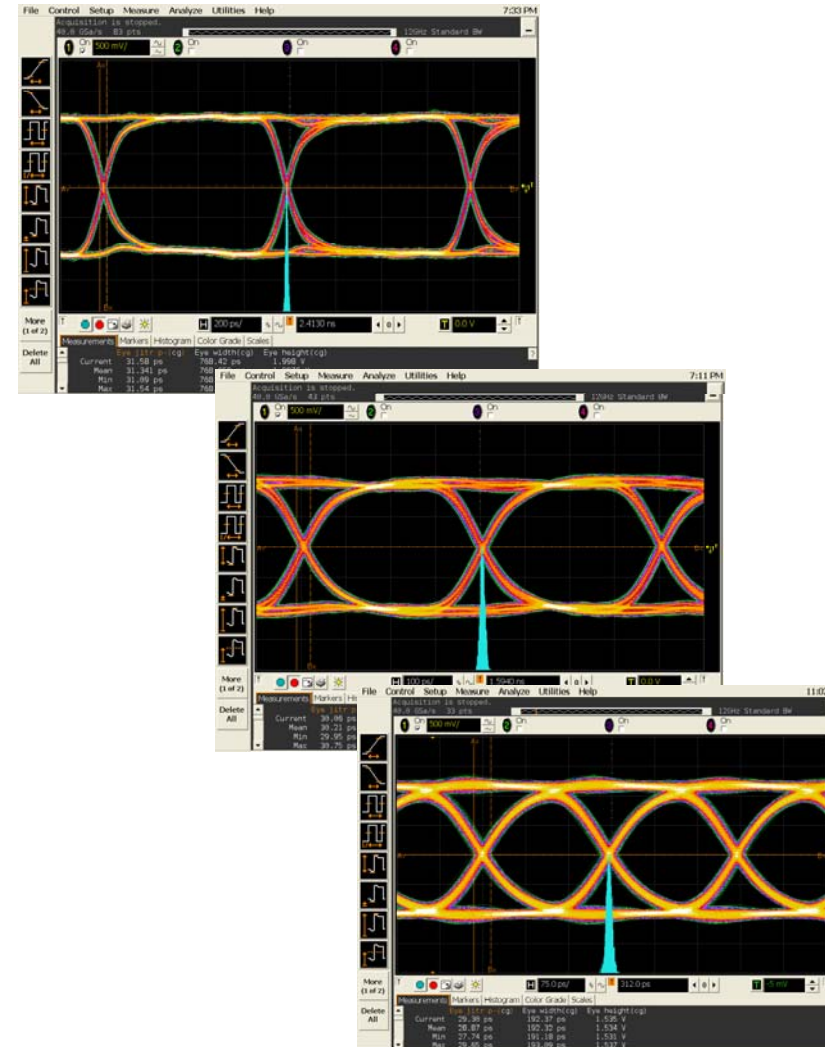
- Business Focus : Mixed-signal IP
- Established: 1998
- Skills: Team with outstanding Mixed-Signal Expertise
- Location: San Jose, CA
- Specialty: Low-power, high performance, mixed-signal CMOS design
- Product Focus: PHYs, SerDes, Transceivers, PLLs, DLLs
- Ownership: Privately held
- Rapid growth in the last few years

Products

- SERDES/PHYs for wide applications and data range
 - MIPI, LVDS, XAUI, GPON, EPON, PCI-E, SATA, SONET
 - 1Gbps to 5Gbps
- High frequency transceivers, up to multi-Gigabit range
 - MIPI, MDDI, DDR2, LVDS, SSTL, HSTL
- PLL and DLL
 - Frequency synthesizer, Spread Spectrum, clock & data recovery
- Available in multiple foundries and processes
 - TSMC, UMC, Chartered, Silterra, Fujitsu, Tower
 - 0.25 micron to 65 nm

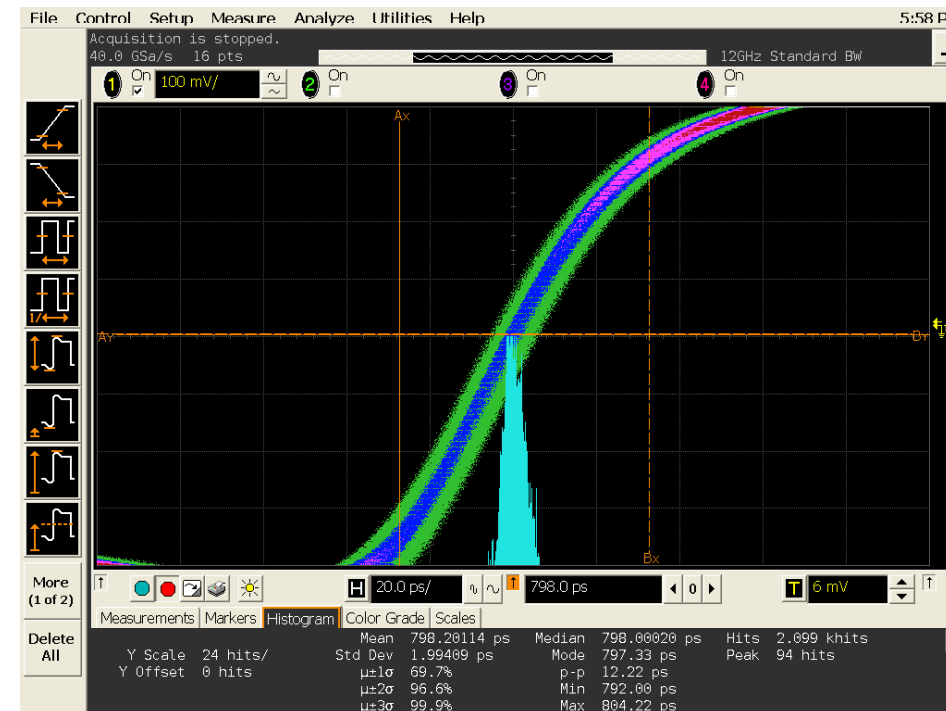
SerDes/PHY

- 1.0 to 4.25 Gbps operation
- Low Power dissipation
- Rx post-equalization enables lower BER/longer distance transmission
- Highly programmable
 - TX pre-emphasis
 - RX post-equalization
 - On-chip RX and TX termination (50, 60, 75 Ω)
 - Voltage swing at high speed serial outputs (175 to 800 mVpp)
 - Data-rate to Reference Clock frequency ratio (4, 5, 8, 10, 16, 20)
- Modular design to facilitate customization (single, Dual, Quad, multiple Quads)



High Performance PLLs

- Programmable high output frequency range up to 2.8 GHz
- Very Low Jitter, < 13ps P-P
- Wide clock input range
- Low power
- Fast lockup time
- Small size



Mixed-Signal IP for Mobile Application

- Low-power
- Up to 1Gbps operation
- Point-to-point differential interface

MIPI D-PHY:

- Supports both high-speed and low-power modes
- Support multiple data lanes and a clock lane, uni-directional and bi-directional operations
- Contributing member of MIPI org.

MDDI: Transceiver

- Second generation with backward compatibility
- Low power Hibernation receiver to minimize standby current
- Close working relationship with Qualcomm and a VESA member

Mixel is the only IP provider with silicon-proven IP for MDDI and MIPI

Deliverables

- Data Sheet
- Characterization data
- GDS II data base
- LVS netlist
- Integration guidelines
- Timing model
- Verilog model
- LEF file
- First-class customer support through transfer to production

Summary

- A growing portfolio of high performance silicon-proven Analog/Mixed-signal IP's in multiple foundries and processes
- IP for a broad range of applications and protocols
 - MIPI, MDDI, XAUI, GPON, EPON, DDR2, Backplanes
- First silicon functionality is the rule, no exceptions
- Exceptional quality, robust designs, resulting in high yield
- Outstanding customer support through transfer to production

Your Mixed-Signal IP Partner

Come Visit us at DAC booth #665



Thank you

- Explore Mixel IP at ChipEstimate.com
- Use Mixel IP to plan your next chip!
- Please stay and talk with Ashraf Takla

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