



Rambus[®]

Greg Tanaka
Sr. Manager

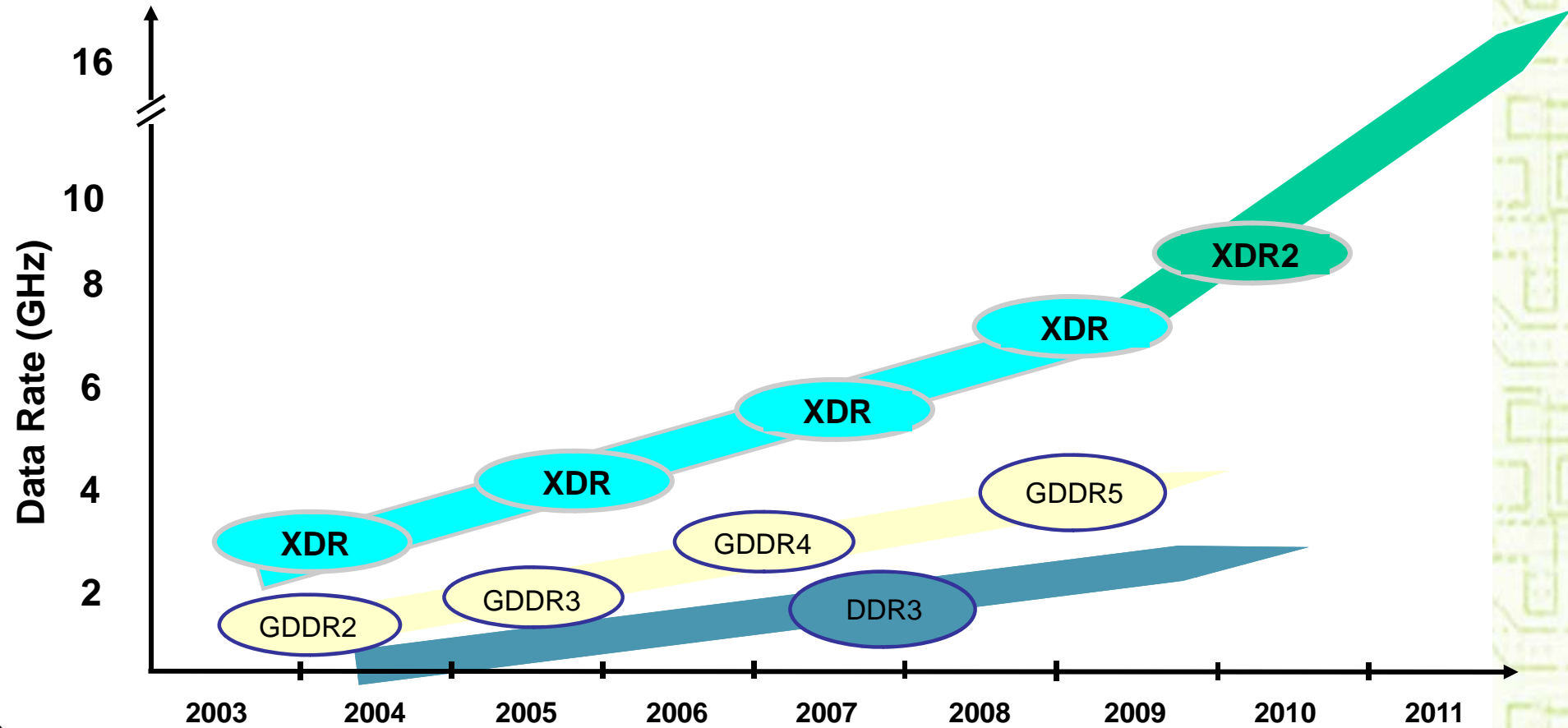
Rambus High-Speed Interface IPs

- Ultra-High Bandwidth XDR Memory
- Serdes
 - PCIe
 - RapidIO
 - XAUI
- Digital Controllers
 - PCIe Gen1 & 2
 - RapidIO
 - SPI4.2
 - Ethernet



XDR vs. Traditional Memory Roadmap Comparison

Rambus



ChipEstimate.com

Highest Yielding Serdes

Rambus

- Designed With Greatest Margin To Spare
- Characterization Goes Beyond Alternative Solutions
 - Total receive jitter tolerance
 - Silicon characterized in real, worst case environments with all process corners
 - Statistical information to tune for highest volume production

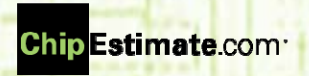
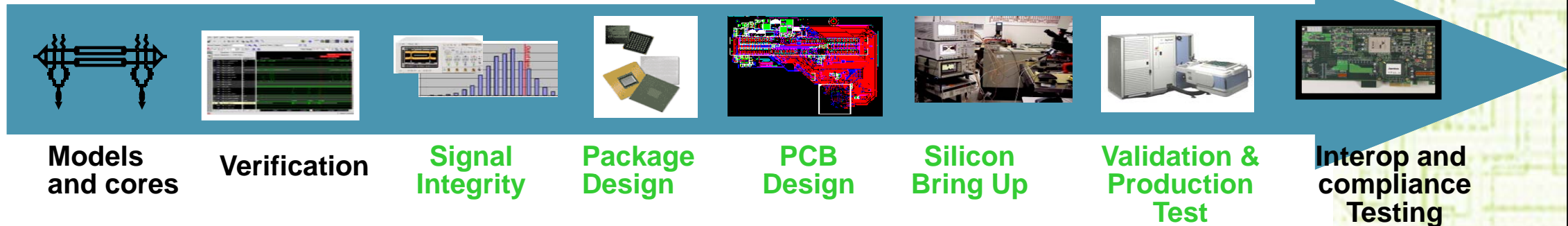


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Highest Yielding Serdes

Rambus

- Designed With Greatest Margin To Spare
- Characterization Goes Beyond Alternative Solutions
- Most Complete Deliverables:



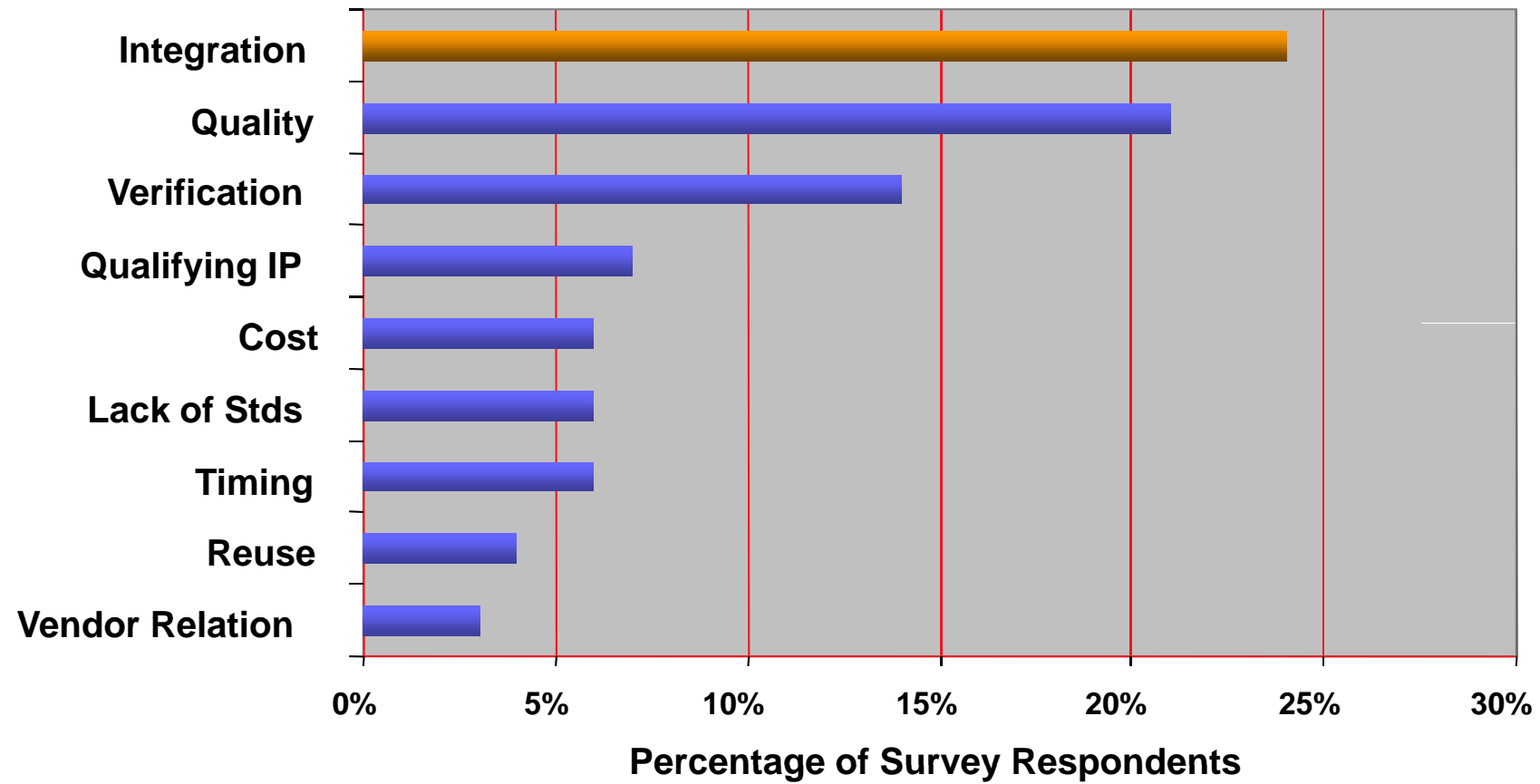
Highest Yielding Serdes

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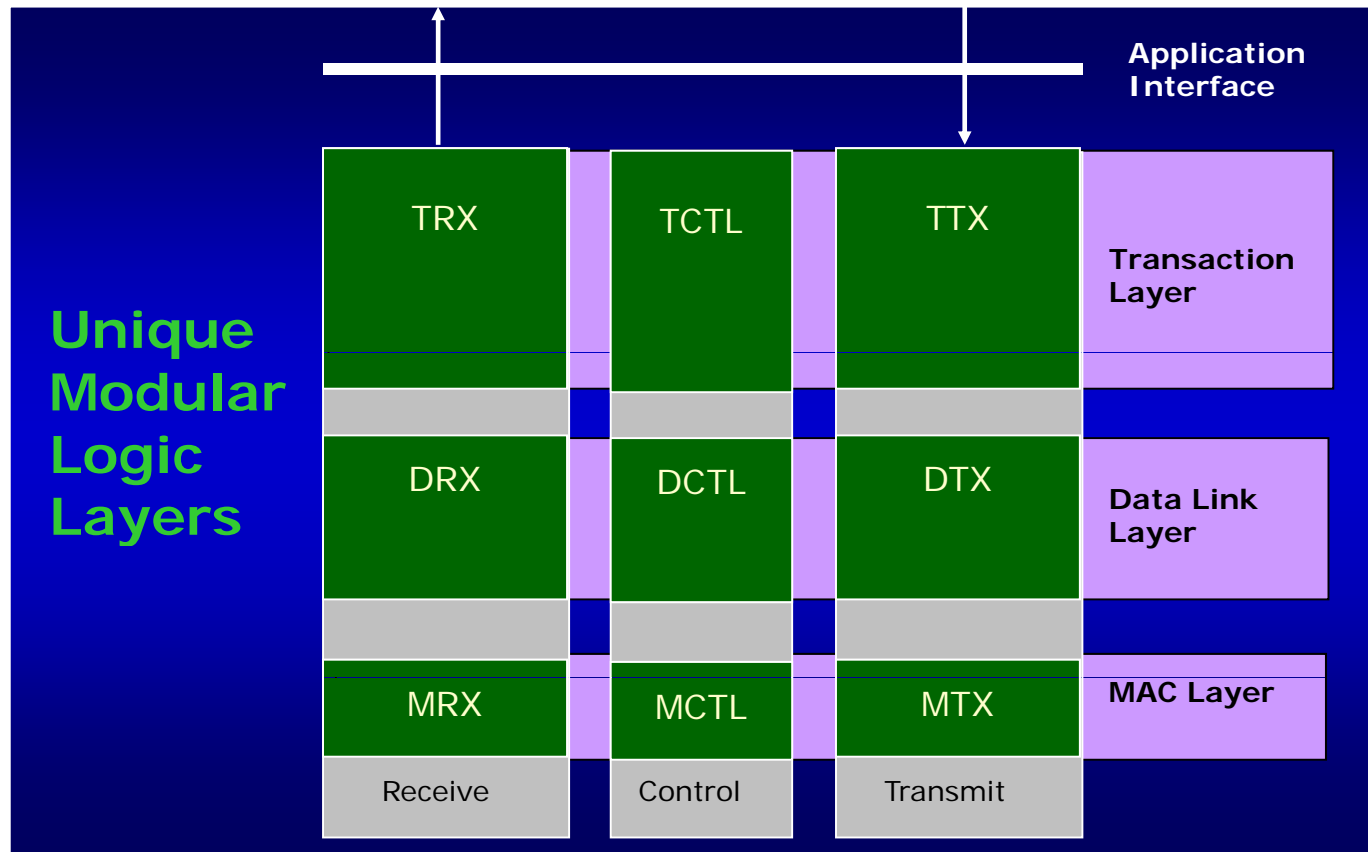
- Exclusive eScope Provides Eye-diagram Of Your Chip In-system
 - Delivers highest accuracy margin data
- Unique High-volume Low-cost Manufacturing Test Features
- Production Proven
 - Millions of chips shipping



IP Challenges Require Flexible Design IP



GPEX Design IP Easiest To Integrate



- Gen 1.1 and 2.0
- I/O Virtualization (IOV)
- Endpoint
- Root Complex
- Dual mode
- Switch port
- Switch
- OCB Bridges
- Multi-Function Support
- Flexible Application I/F
- 32 to 128 Bit Datapath



GPEX IP Differentiation

- **Perfect Fit** for Your Application Layer Interface
 - IP Designed To Interface Directly To Your Design
 - Fastest Integration And Shortest Time-To-Market
 - Design Services For Customized Interfaces Tailored Exactly For Your Design
- **Most Configurable** Endpoint, Root Complex, Hybrid, Switch And Switch Port Solutions
 - Configurable Per Specific Customer Application Requirements
 - Design Aware Solutions For Maximum Quality of Results
 - GUI Tool For Quick Configuration And Area Optimization



Thank you

- Explore Rambus IP at ChipEstimate.com
- Use Rambus IP to plan your next chip!
- Please stay and talk with Greg Tanaka

