



# **SARNOFF EUROPE ESD DESIGN SOLUTIONS**

**Katty Van Mele  
Benjamin Van Camp**

# SARNOFF EUROPE ESD DESIGN SOLUTIONS

- **Enable to integrate ESD design solutions in custom IO/IC, economically and without performance compromises**
  - Faster time to market
  - Smallest silicon area layout
  - Optimized ESD and IC performance
  - Lower R&D/IP risk and expense
  - Easy integration and adoption
  - Quality solutions and support
- **TSMC Design Center Alliance partner (DCA)**
- **UMC IP Alliance partner**



# SARNOFF EUROPE ESD DESIGN SOLUTIONS

- Robust track record in IDM – Fabless – Foundry business



- Product proven in 8 CMOS generations, BiCMOS, BCD...
  - Since 2002: 433 volume production ICs released
  - In 2007: 19 ICs released in 65nm CMOS
  - Announcing 40nm silicon proven solutions by August 2008



# Trends in IC design – Impact on ESD

- Cost and complexity of next generation IC development
  - Differentiation: features, performance, time-to-market
- ... driving the need for fast design cycles, IP re-use and design portability
- Impact on ESD: each IC requires flexible, easy-to-integrate, product proven, portable ESD solutions which do not compromise the circuit performance



# ESD design enablement

- **Product proven, portable ESD design becomes an enabler of competitive differentiation**
  - Enable best IC functionality and performance
    - High speed/RF: low capacitance and zero resistance signal load
    - Flexible: solutions for any custom circuit or requirement
    - Economic: smallest silicon area layout
  - Enable volume ramp and production on different processes
    - Product proven solutions
    - Clean IP mitigating infringement liabilities
    - First time right ESD design
- **Sarnoff Europe ESD design solutions and tools drive critical success factors in advanced IC design**



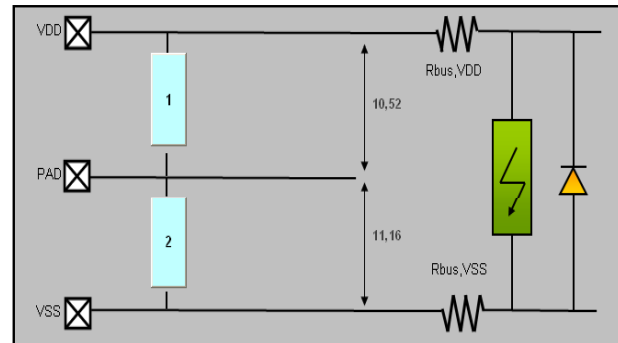
# ESD design enablement – TakeCharge

- We match our offer to the customer needs
  - **TDS – TakeCharge Design Solution**
    - One IC/one problem solutions
    - Fast turnaround in less than 3 weeks
  - **TDK – TakeCharge Design Kit**
    - Custom design tool for multiple IC per process
    - Full solution package
    - Readily available for major foundries in 0.18um to 65nm CMOS
    - 40nm CMOS TDK available from August 2008
  - **TakeCharge Maintenance**
    - Product implementation support
    - Tool and technology updates

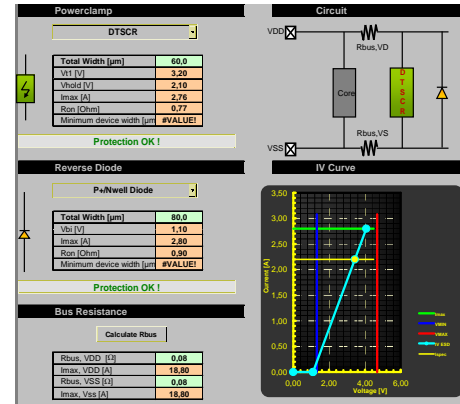


# TakeCharge Design Kit – Solutions and tool

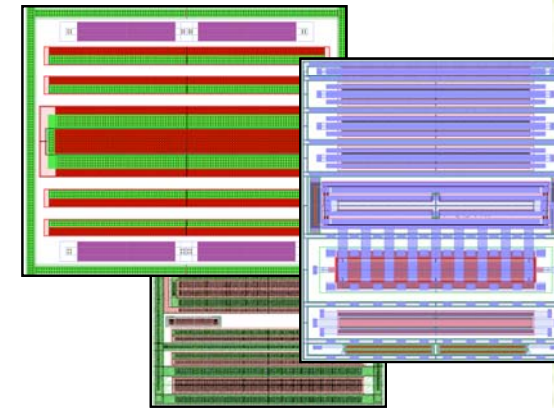
## solution selection



## optimization



## GDSII reference cells

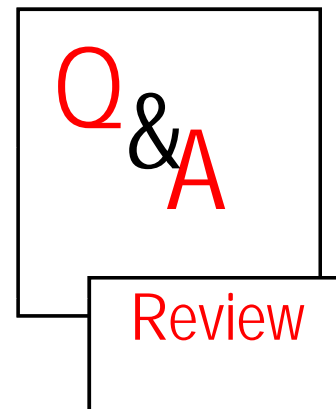


## training

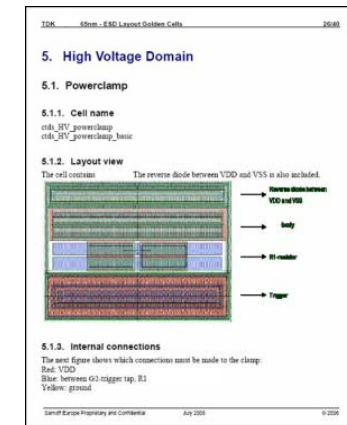
Dual diode protection	Full local protection	Semi local protection	Secondary protection	Self protective drivers
<ul style="list-style-type: none"> <li>+ Most area efficient protection</li> <li>+ Low capacitance</li> <li>+ Linear capacitance</li> </ul>	<ul style="list-style-type: none"> <li>+ Safe local clamping</li> <li>+ Bus resistance is NOT critical</li> </ul>	<ul style="list-style-type: none"> <li>+ Safe local clamping for NMOS driver/GOX</li> <li>+ Bus resistance is NOT critical</li> </ul>	<ul style="list-style-type: none"> <li>+ Use ESD performance of the drivers</li> </ul>	<ul style="list-style-type: none"> <li>+ Use ESD performance of the drivers</li> <li>+ No diodes needed</li> </ul>
<ul style="list-style-type: none"> <li>- Bus resistance impacts ESD protection efficiency</li> </ul>	<ul style="list-style-type: none"> <li>- Large area consumption to locally clamp every I/O pin</li> <li>- Large capacitance</li> </ul>	<ul style="list-style-type: none"> <li>- Large area consumption</li> <li>- Large capacitance</li> <li>- No solution for PMOS driver in IO case</li> </ul>	<ul style="list-style-type: none"> <li>- Separate diodes needed</li> <li>- Isolation resistance influences normal operation</li> </ul>	<ul style="list-style-type: none"> <li>- Large area</li> <li>- Large junction and gate capacitance</li> </ul>
<b>To be used for</b> <ul style="list-style-type: none"> <li>• LV input only</li> <li>• HV input only</li> <li>• Primary protection in combination with resistance for LV outputs</li> </ul>	<b>To be used for</b> <ul style="list-style-type: none"> <li>• LV input only</li> <li>• HV input only</li> <li>• Secondary protection in combination with isolation resistance</li> </ul>	<b>To be used for</b> <ul style="list-style-type: none"> <li>• LV input only, OVT</li> <li>• HV input only, OVT</li> <li>• RT SCR protection</li> <li>• ESD-on-SCR protection</li> </ul>	<b>To be used for</b> <ul style="list-style-type: none"> <li>• LV outputs</li> <li>• Drivers or small local clamps act as secondary protection</li> </ul>	<b>To be used for</b> <ul style="list-style-type: none"> <li>• Large LV outputs</li> </ul>

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## engineering support



## documentation



# Thank you!

- **Explore SARNOFF EUROPE IP at [ChipEstimate.com](http://ChipEstimate.com)**
- **Use SARNOFF EUROPE ESD DESIGN SOLUTIONS to plan your next custom IC design!**
- **Please stay and talk with Katty and Benjamin**
- **Visit us any time at our booth number 334**

