

Dan Kochpatcharin
Deputy Director, IP Portfolio Marketing

Design Infrastructure Support

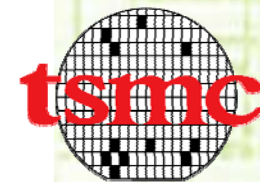
- Active Accuracy Assurance (AAA) Initiative
 - Accuracy-Centric Design Support Data
 - Model Accuracy
 - Tool Qualification
 - Comprehensive PDK
 - Efficiency-Centric Design Methodology
 - SoC Design Platform
 - Low-power Approach
 - Quality-Centric IP/Lib Portfolio Support
 - Availability
 - Quality
- Complementary Design Service Support

IP Strategy

- Accelerate the development of IP ecosystem
- Implement TSMC internal operation as “enabler”
- Set first priority on foundation IP (standard cell, memory, standard I/O) development
- Provide TSMC validated “enablement circuits” to ecosystem partners for fast IP development
 - E.g. Serdes, Osc, PLL, DLL, Bandgap Ref, VCO, etc.
- Complement ecosystem partner in foundation IP and application IP development

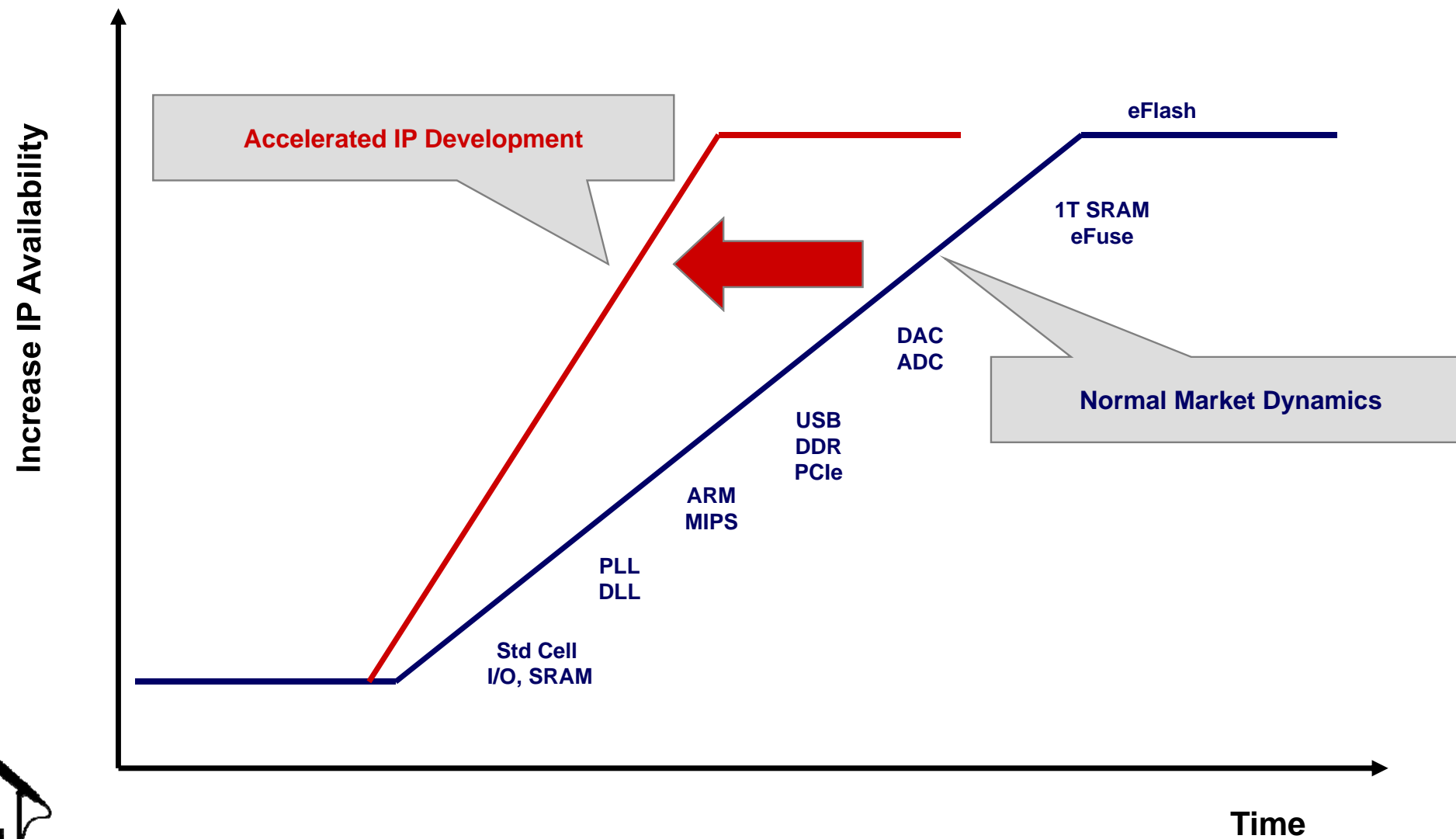


Re-optimize IP with the process evolution

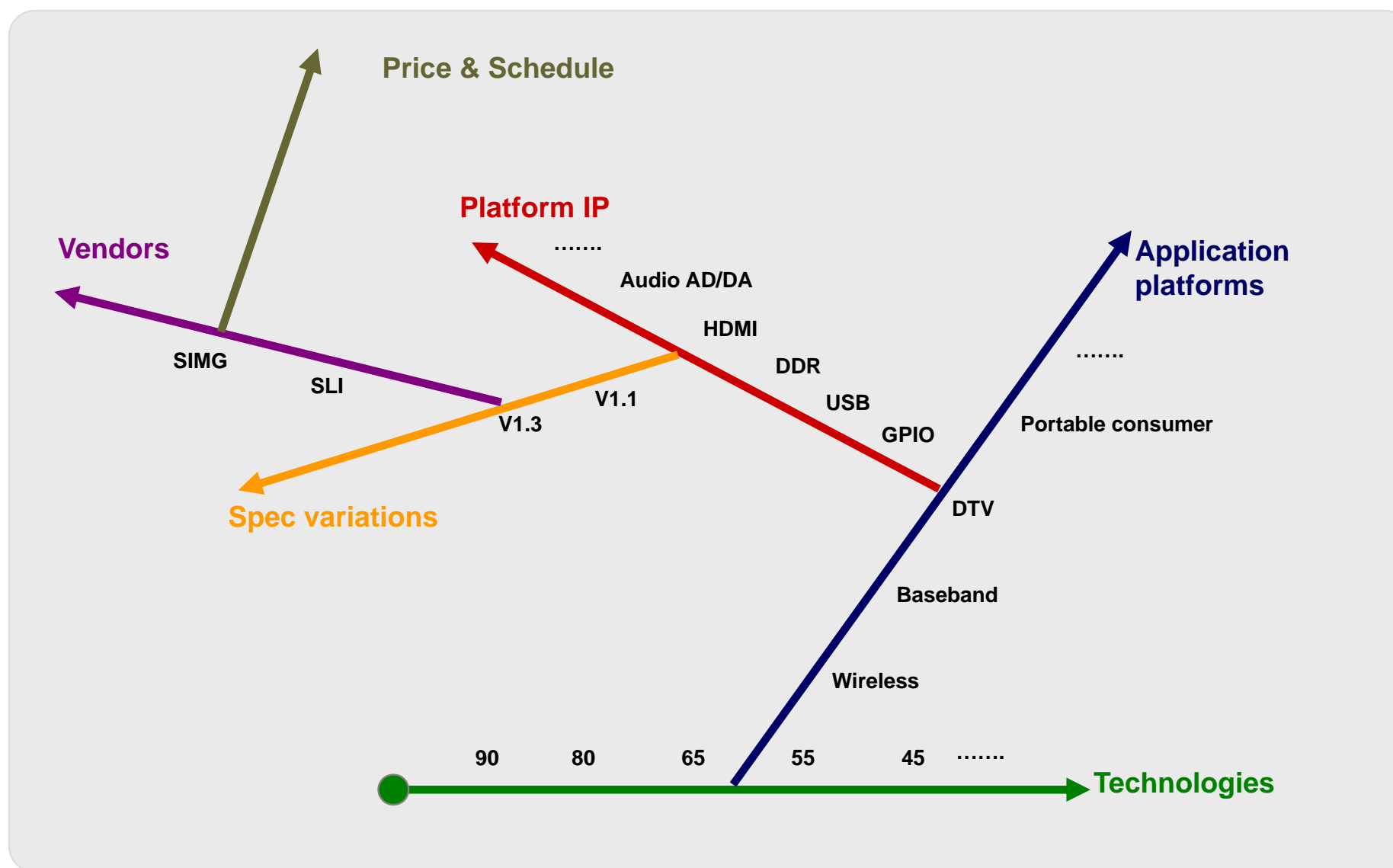


TSMC Property

IP Strategy → Development Acceleration

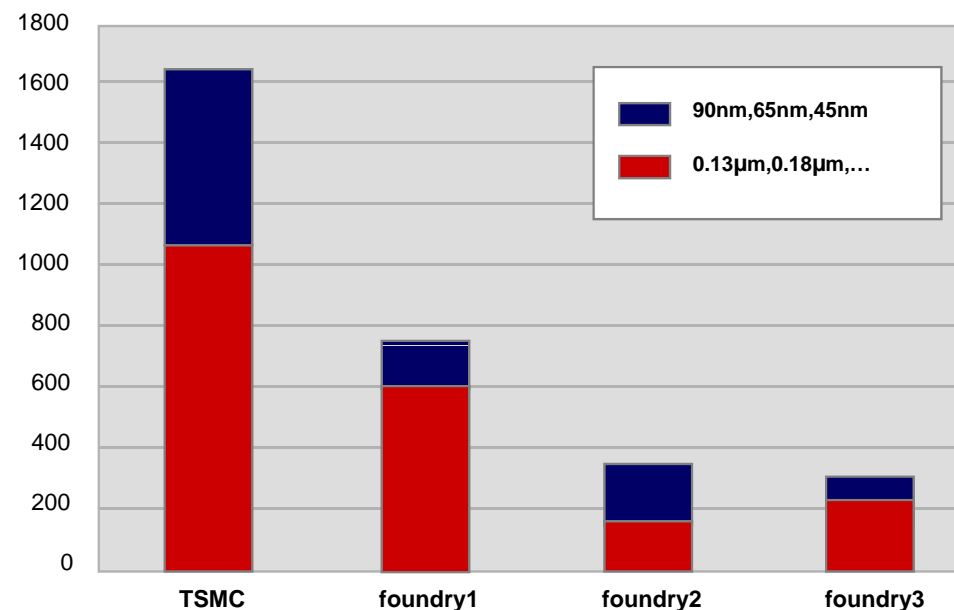


IP Strategy → Many Considerations



Most Comprehensive IP Portfolio

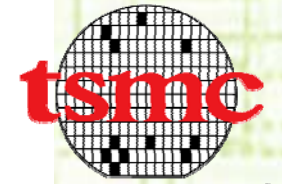
Over 1600 IP from 40+ vendors including TSMC
 Closest competitor has less than half
 Proper balance between advanced and mainstream portfolio



Source: Chip Estimate, Design&Reuse, TSMC



Segment Focus



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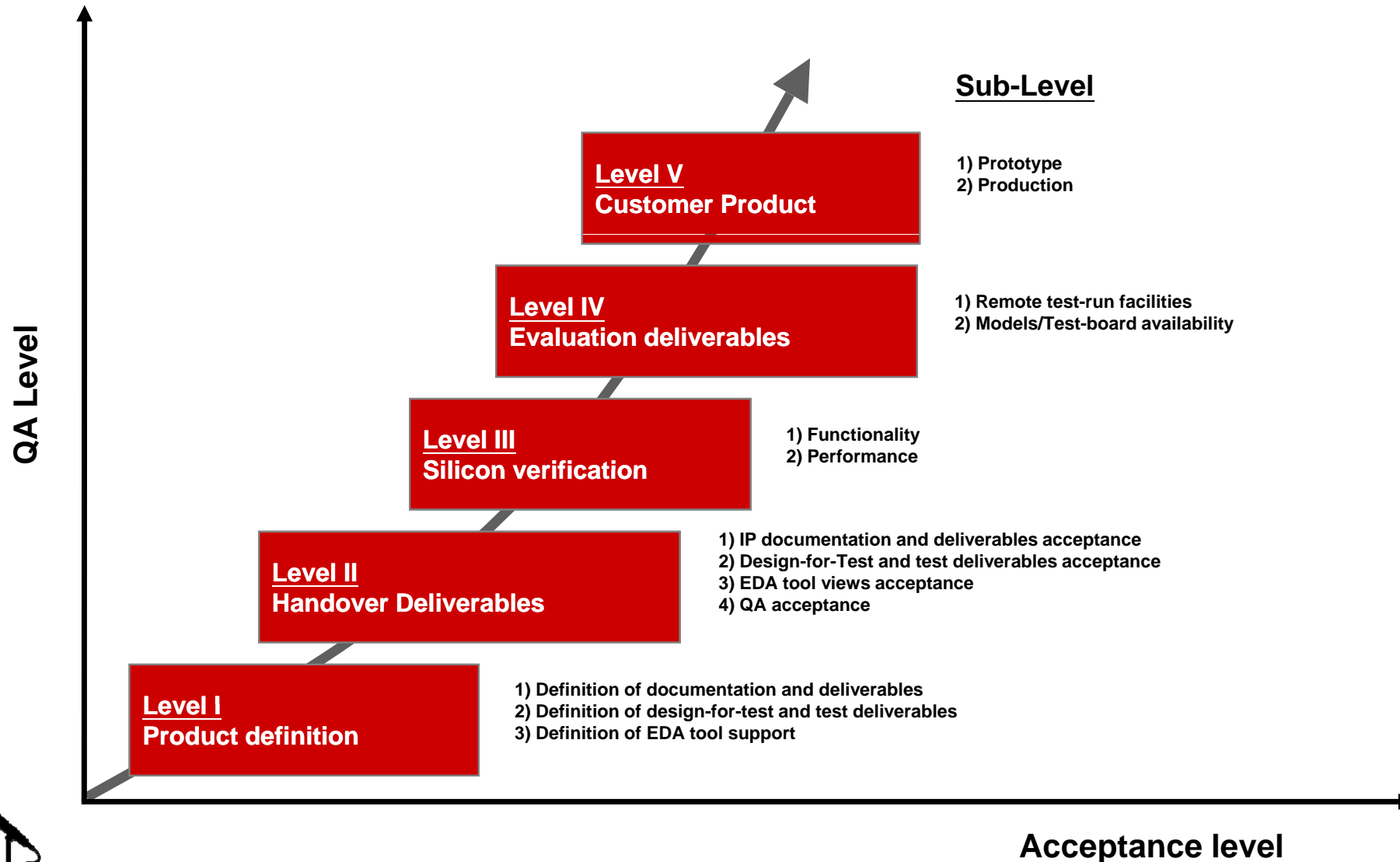
		LP Focus Segments			G/GT/GP Focus Segments	
IP Categories	IP List	Mo bile Cel lula r	Porta ble Consume r	Wireless	Digital Home	Digital Office Data Center
Foundation Library/IP	Standard Cell	✓	✓	✓	✓	✓
	Memory Compilers	✓	✓	✓	✓	✓
	GPIO, 2.5V -> 1.8V OD 3.3V	✓	✓	✓	✓	✓
	800MHz~1GHz -> 2-3G PLL	✓	✓	✓	✓	✓
Memory Interface	SD/MMC I/O	✓	✓	✓	N/A	N/A
	Mobile DDR I/O	✓	✓	✓	N/A	N/A
	DDR2 -> DDR3 Phy	N/A	N/A	N/A	✓	✓
High Speed Interface	DLL	N/A	N/A	N/A	✓	✓
	USB2.0 OTG Phy	✓	✓	✓	✓	N/A
Storage Interface	PCI-e Gen 1/Gen 2	N/A	N/A	✓	✓	✓
	SATA 1.5G/3G -> 6G	N/A	✓	✓	✓	✓
Display	MIPI Phy	✓	N/A	N/A	N/A	N/A
	HDMI Tx/Rx	✓	✓	N/A	✓	N/A
	LVDS Tx/Rx	N/A	N/A	N/A	✓	N/A
Networking	LVDS I/O	N/A	N/A	N/A	N/A	✓
	Xaui/Double Xaui	N/A	N/A	N/A	N/A	✓
	10-12.5Gbps Serdes	N/A	N/A	N/A	N/A	✓
	TCAM	N/A	N/A	N/A	N/A	✓
Embedded Memory	OTP/ MTP	✓	✓	✓	✓	✓
	Electrical Fuse	✓	✓	✓	✓	✓
	Emb DRAM	✓	✓	N/A	✓	✓


















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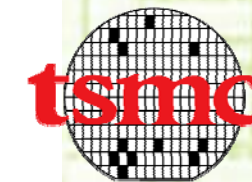
QA Acceptance Level



Compliance Status on TSMC-Online

Compiler Name	Description	Cell Size (um ²)	TSMC comment	Level I	Level III	Level IV	Level V
tsmc90g_sram-sp-hs_TBD	HS-SRAM-SP	1.27	DRM v0.1				
tsmc90g_sram-sp-hs_2002q4v0	HS-SRAM-SP	1.27					
tsmc90g_sram-dp-hs_2002q4v0	HS-SRAM-DP	2.2344					
tsmc90g_sram-dp-hs_2003q2v1	HS-SRAM-DP	2.2344					
tsmc90g_rf-sp-hs_2002q4v0	HS-RF-SP	1.27					
tsmc90g_rf-dp-hs_2002q4v0	HS-RF-2P	2.2348					
tsmc90g_rf-dp-hs_2003q2v1	HS-RF-2P	2.2333					
tsmc90g_rom-diff-hs_2002q4v0	HS-dROM	0.18					

The purposes of TSMC's validation works performed on memory libraries are only to clarify that specifications of such memory libraries are compatible with specifications of TSMC's manufacturing technology environment. **TSMC DO NOT AND WILL NOT ASCERTAIN, AND SHALL NOT BE HELD RESPONSIBLE FOR THE QUALITY, FUNCTION OR PERFORMANCE OF SUCH MEMORY LIBRARIES.** [TOP](#)



TSMC Property

Tight Screening for Quality

● Pre-screen

- # IP: 1052
- Failure rate: 9.2%

● Level-I

- # IP: 982
- Failure rate: 11.8%

● Level-III

- # IP: 85
- Failure rate: 52.2%

Summary

Type	Pre-screen			Level-I			Level-III		
	Library /IP count	Lib/IP passed	Fail IP/Lib %	Library/IP count	Lib/IP passed	Fail IP/Lib %	Library/IP count	Lib/IP passed	Fail IP/Lib %
Library	509	462	9.2%	498	452	9.2 %	30	6	80.0 %
SRAM	216	162	25.0%	203	165	18.7 %	81	43	46.9 %
Other Memory	300	295	1.7%	286	279	2.4 %	48	22	54.2 %
IP	133	133	0.0 %	127	86	32.3 %	19	14	26.3 %
Total	1158	1052	9.2 %	1114	982	11.8 %	178	85	52.2 %

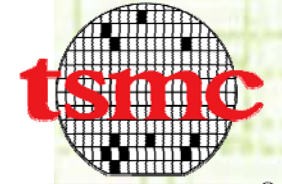


Summary

- Comprehensive IP support from IP Vendors
- Quality
- Partnership Focus with IP Vendors

Thank you

- Explore IP developed for TSMC at ChipEstimate.com
- Use TSMC foundry to plan your next chip!
- Please stay and talk with Dan Kochpatcharin



TSMC Property

