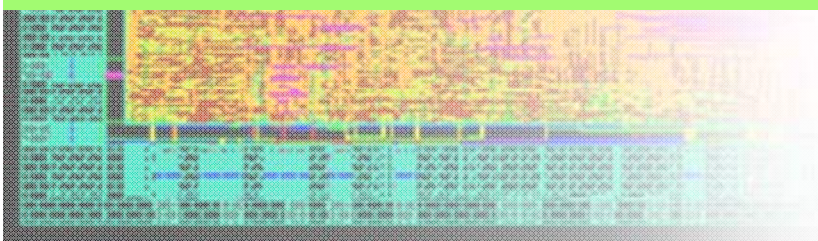


denali

Denali DDR PHY: Flexibility and Speed

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Sr. Technical Marketing Engineer



DDR Memory: a Big, Common Problem



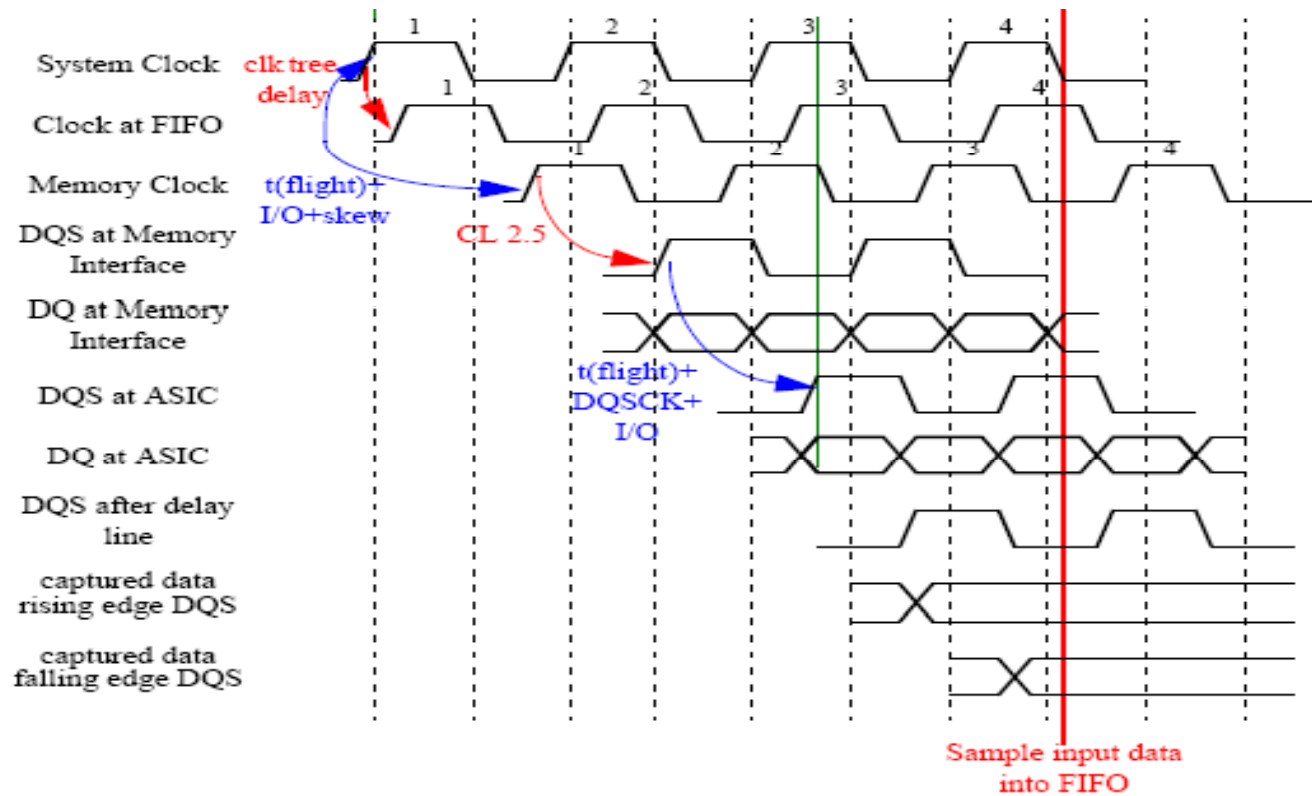
- DDR memory is now on the majority of SoCs
- DDR PHY creation and timing closure paces the chip schedule
 - Hundreds of highly skilled engineering hours
 - Large toolset needed
- It's much more than connecting a DLL and IO pads!!
- PHY speeds are rapidly increasing, and timing closure is getting geometrically harder



Why is the PHY difficult?

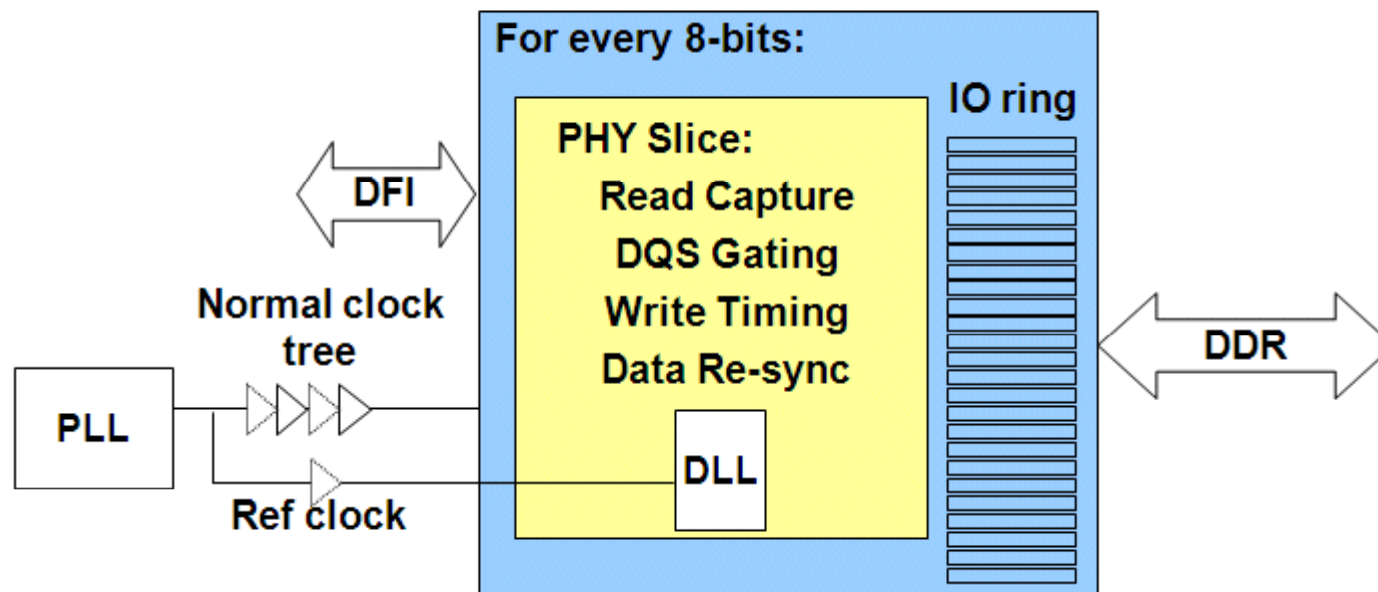


- Tight timing margins
- Wide busses, large skews, much SI noise
- Explaining how multiple clock domain timing and layout works to the EDA tools
- Controlling latency
- Proving that the PHY design will work

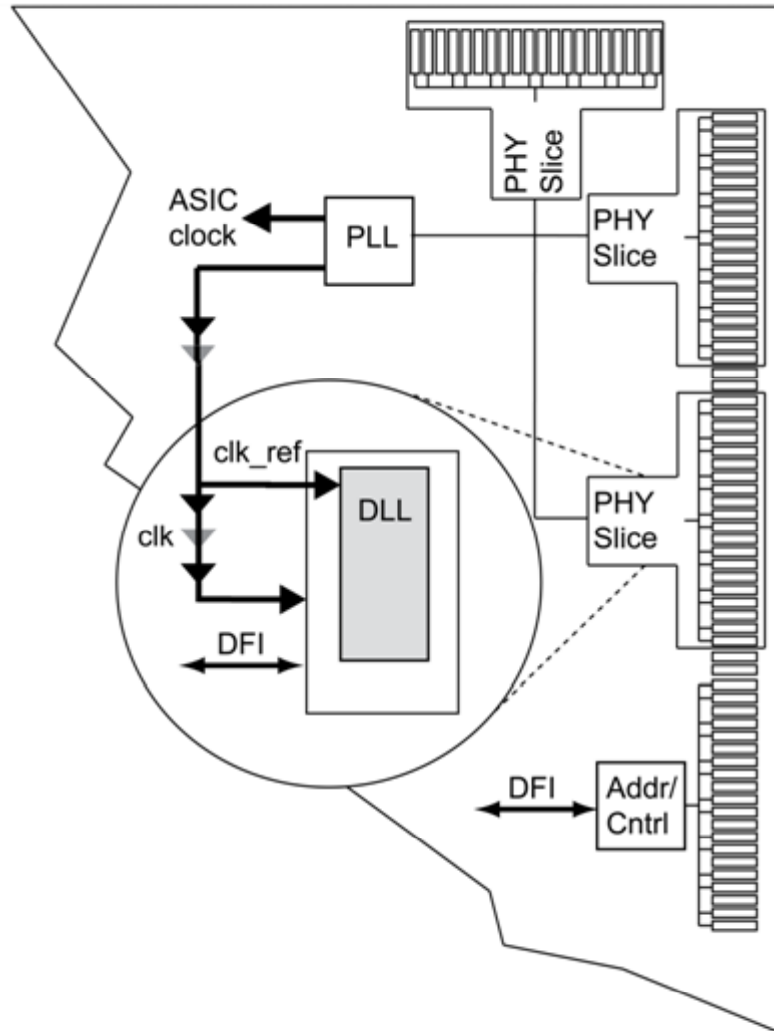


PHY Architectural – Data slice

- Separate PLL
 - Use for multiple PHY Slices
 - Can use for rest of chip
- Hardened 8-bit PHY Slice
 - Highly reusable
 - Fully timing closed
 - GDSII
 - Main engine of the PHY
- I/Os integrated at RTL level
- Pad vendors:
 - TSMC
 - ARM
 - Aragio
 - Dolphin
 - Analog Bits



PHY Physical Structure



- Flexible structure
- Harden slice then PHY
- Very adaptable to different floor plan needs
 - Chip size
 - Pad type, package type
 - Bus Width
 - Power/ground ratios
 - DLL does not require special power due to built-in isolation
 - ESD strategies



PHY Architectural Choices

- Overall architecture
 - Designed for reuse
 - Proven in more than 100 customer designs
 - Denali's 3rd generation PHY
 - Highly flexible and highly tunable
 - 1X Clock, multiple DLLs

***Every tuning option is a
“Get out of Jail Free” card...***



Key Points of the DDR PHY Solution



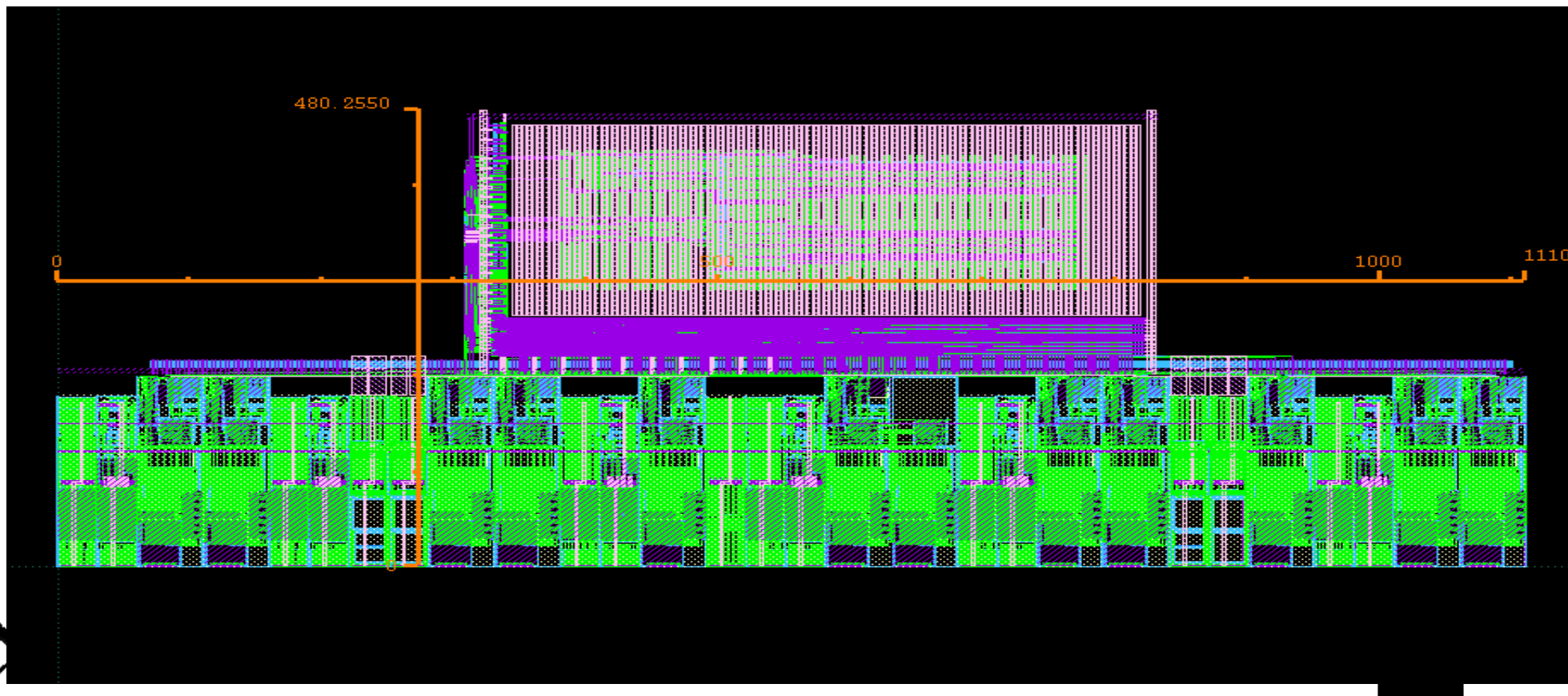
- Configurable
- Complete IP delivery
 - Logical views: RTL/models for simulations and tuning
 - Physical views for floorplanning and implementation
 - All scripts, constraints, .lib files and users manual
- Flexible
 - Integrate to different I/O pads
 - Adaptable to different chips and fab processes
- Denali brings complete domain knowledge and eco-system
- Built on proven, high quality technology platform
 - Built on Databahn configurable platform, which has produced 250+ designs, 100+ in silicon (**100% success**)





Denali PHY Physical Design Flow

- Example Chartered 65G data slice with pads
- Denali DDR3 PHY IP available now with full support of leveling for DIMMs
- Design kits with best practice layout scripts



Summary



- Denali PHY architecture is silicon proven in more than 100 Denali customer PHYs
- Denali team has extensive PHY hardening experience
- Denali's DDR3 PHY can be hardened by your team with help from Denali best layout practices scripts
- Denali can provide a DDR3 PHY with more flexibility and less risk than our competitors



Thank you

- Explore Denali IP at ChipEstimate.com
- Use Denali IP to plan your next chip!
- Please stay and talk with Rayfes Mondal

The logo for Denali, featuring the word "Denali" in a stylized, cursive font. The "D" is red, and the rest of the letters are blue.