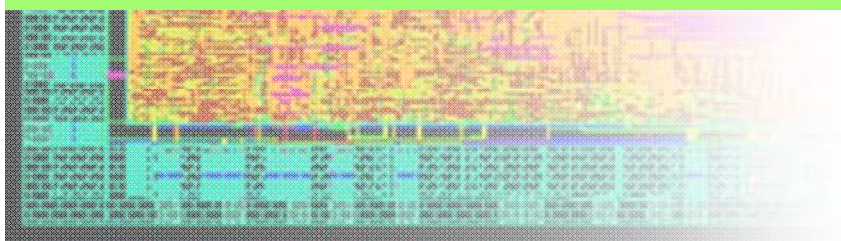


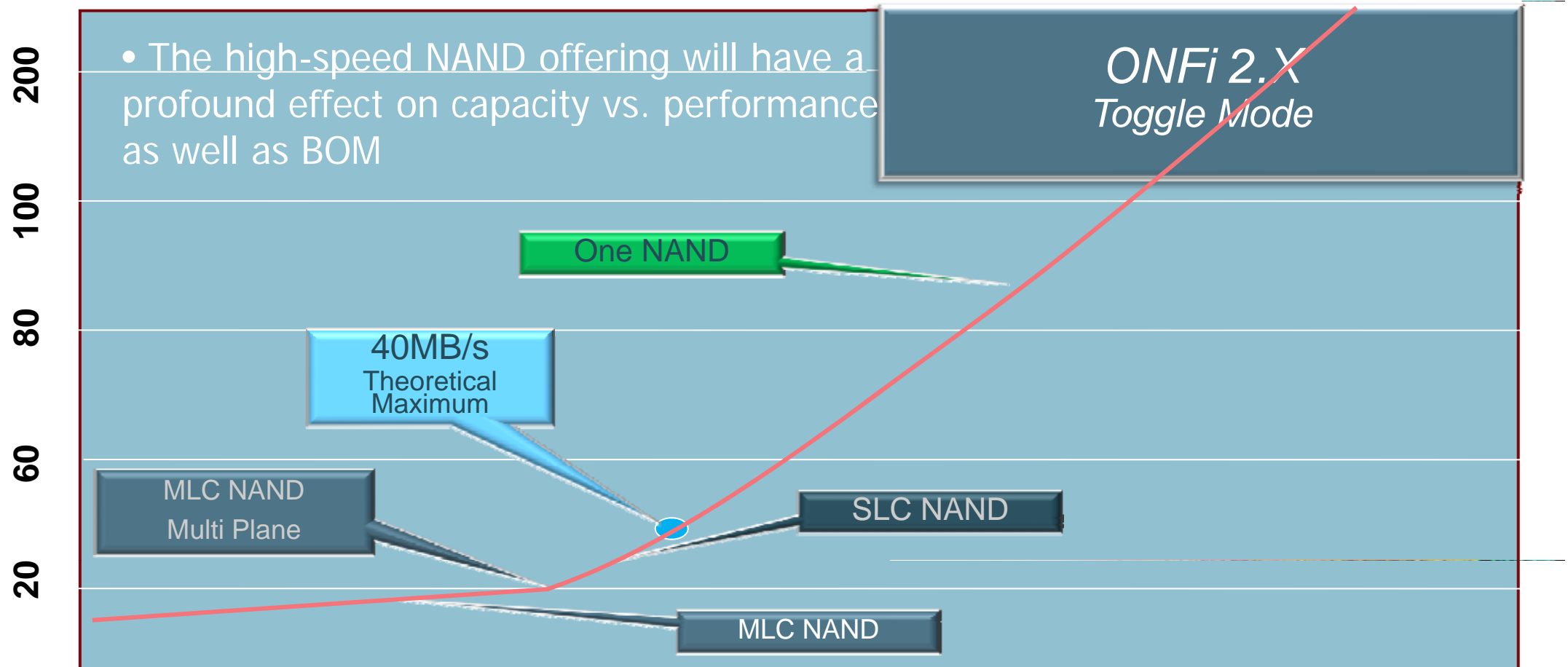
High-Speed Flash: Problem Resolution

Bob Pierce

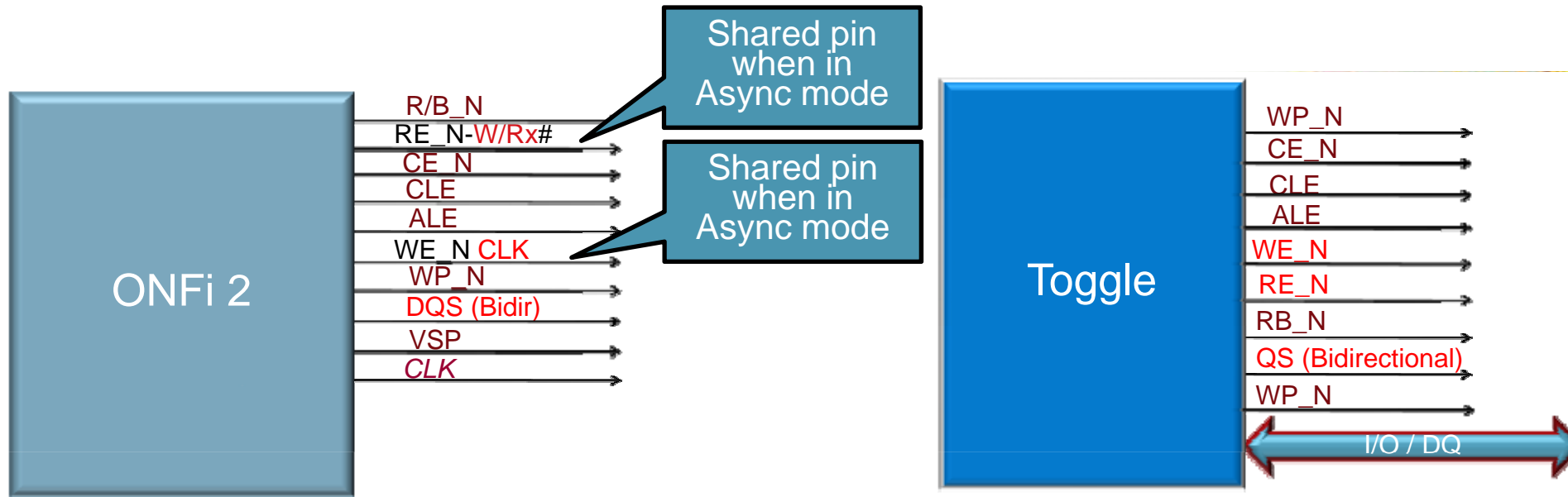
Sr. Director Flash Products



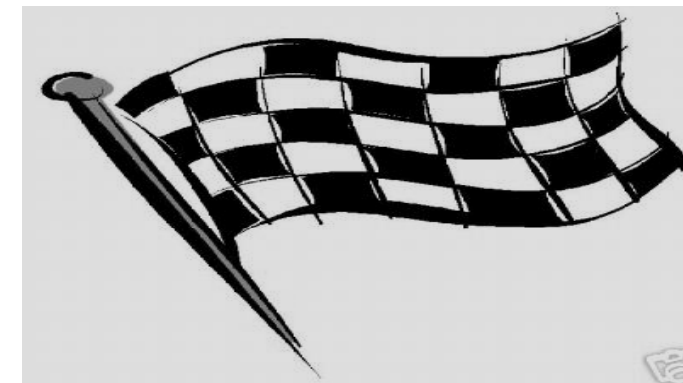
History of NAND Bandwidth Trend



High-Speed Interfaces



- 2 solutions
- Major differences
 - Clock vs. Strobe
 - ONFi CLK and W/R
 - Toggle uses WE_N and RE_N
 - DQS (Bidirectional)
 - 16 bit bus support for ONFi 2



Page Size Impact ???

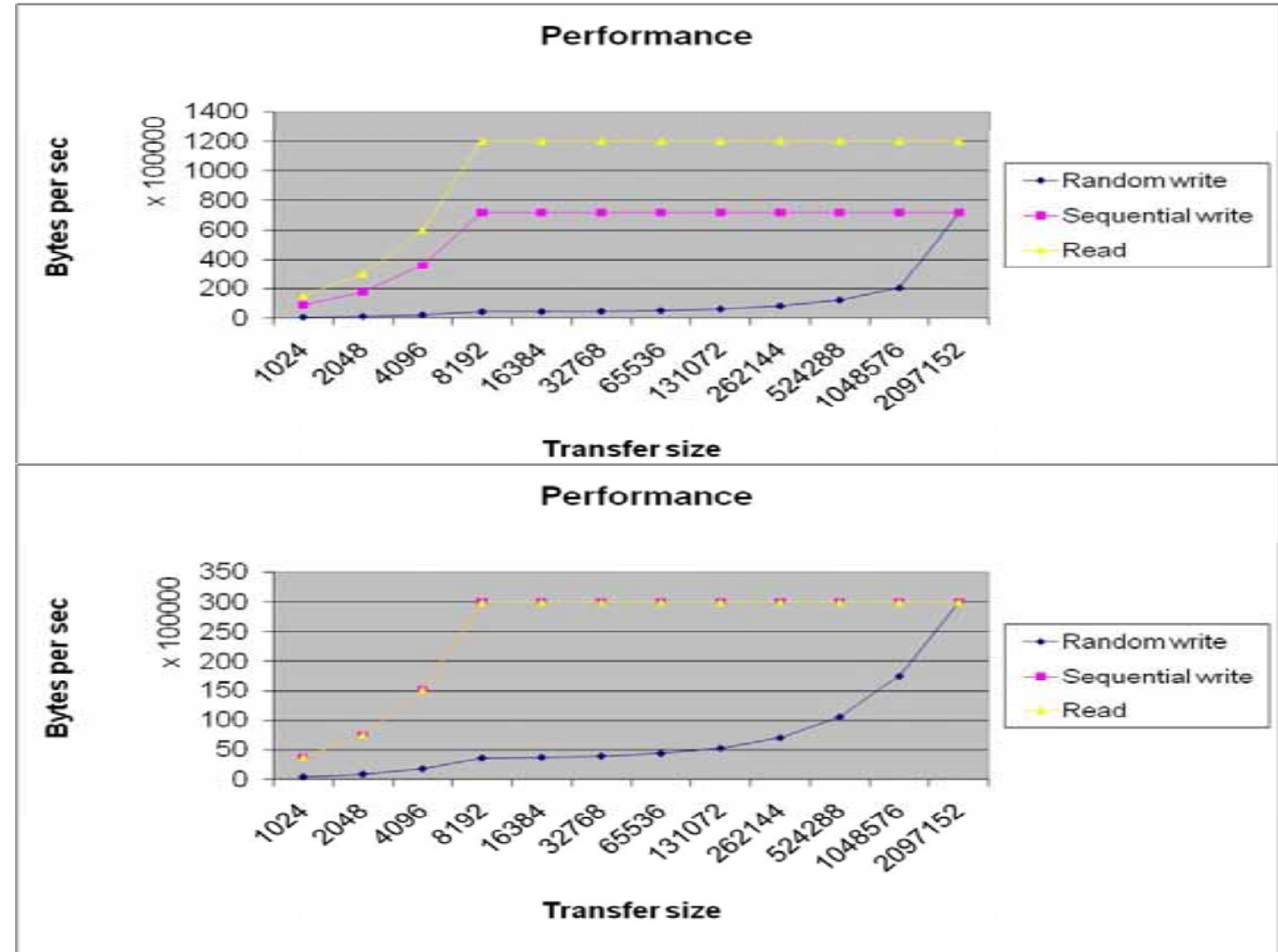
- Transfer time due to large page size
 - For asynchronous devices with 20ns cycle time, you need 160us to transfer 8KB page from controller to device.
 - For read operations where the flash array load time is small (25-50us), this is a very large number impacting performance
- Synchronous DDR interfaces defined to support up to 200MT/s (ONFi2.1 & Toggle)
 - Takes 40us to transfer 8KB page from controller to device
- Impact on random performance
 - Device manufacturers are providing multiple independently addressable dies
 - Flash controller implementations should provide the ability to use these independent dies in parallel
 - Flash controller software should take care of appropriate assignment of data to various blocks to increase parallelism

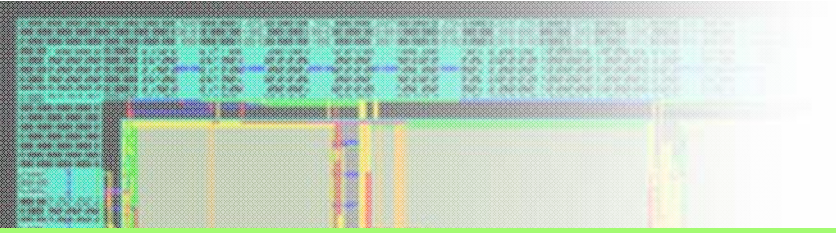


Performance Impact

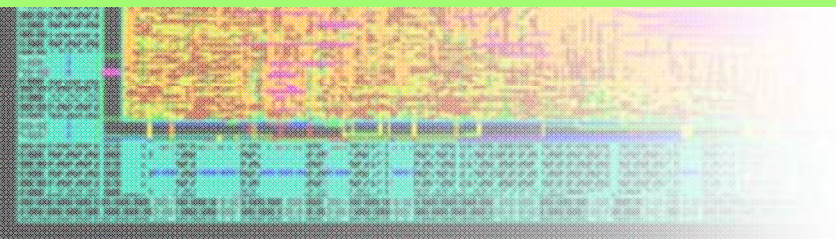
- Toggle-based MLC NAND
- Single controller
- 4 CE
- 8K page size

- Asynchronous MLC NAND
- Single controller
- 4 CE
- 8K page size





ONFi 2, Toggle PHY Overview

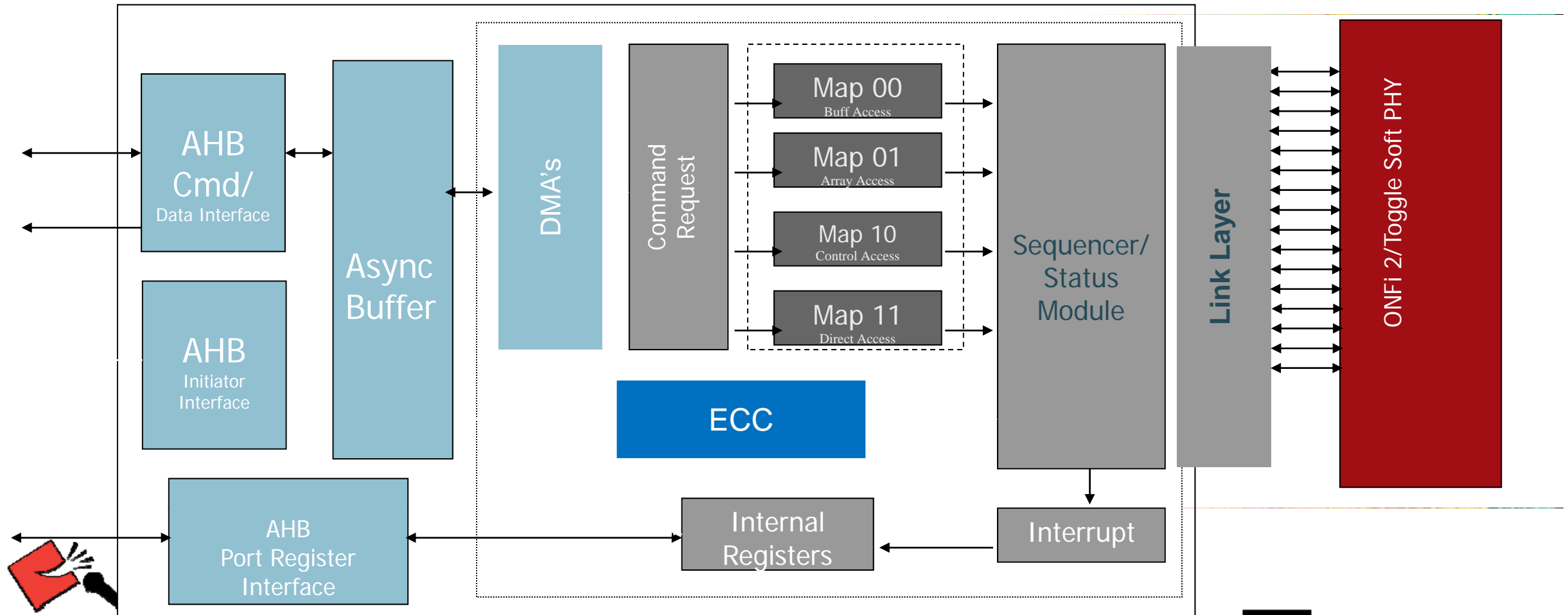


Why A PHY?

- New flash interfaces such as ONFi 2 and Toggle require a controlled timing interface
- Impedance matching is much more important
- Multiple/selectable drive strengths
- Bus turn-around timing (ready-busy, CE)
- Legacy support
- Limited data capture window
- Power management

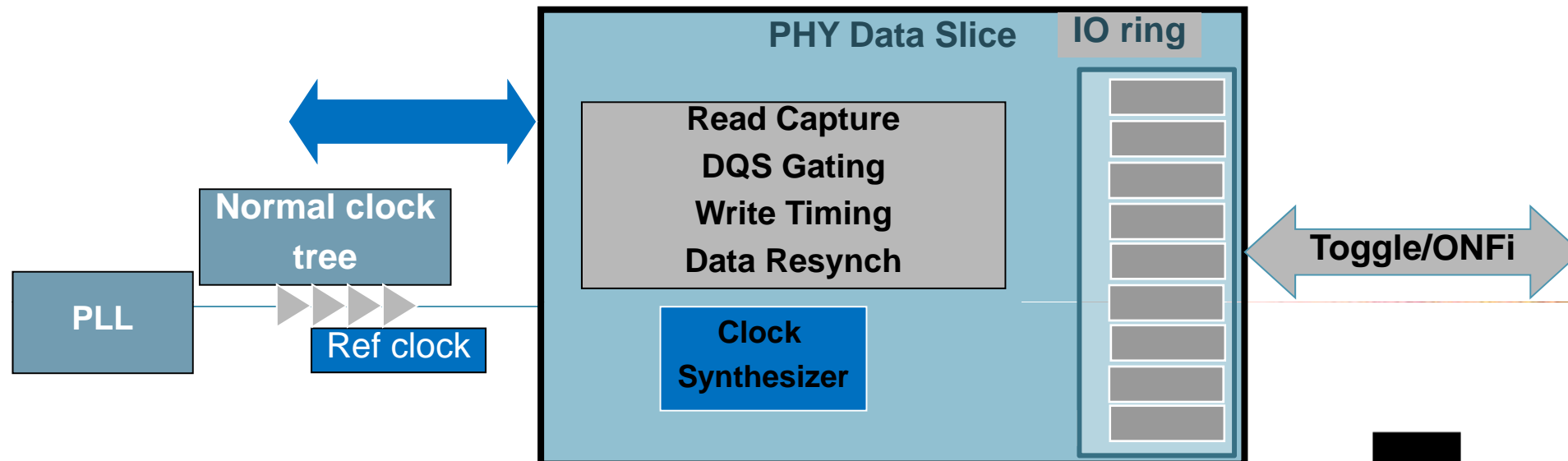


Nand Controller with PHY Support



PHY Architectural Overview

- Separate PLL
 - Use for multiple slices
 - Soft PHY slice
 - Highly reusable
 - Test Logic for at-speed test
 - No DLL reduces power and gate count. 4X clock at IO frequency
- Clock reference
 - Minimally buffered PLL input to slice for source synchronous domain
 - Normal clock tree for DFI, flop-to-flop timing



Soft PHY Solution

- Works with ONFi2 and Toggle
- Base design has been verified by DDR DRAM controller
- Process technology agnostic
- Scalable to many multiple channels
- By-pass mode for async support (Legacy)
- Multiple drive strength support for new high-speed device
- No DLL, simplified clocking methodology
 - No 3rd party core IP
 - I/O's need to be supplied
 - 4X 50/50 Duty clock needed



Conclusion

- Changes in flash technology will require more IP solutions to achieve the performance potential of high-speed NAND devices
- New flash architectural changes will segment the market
 - Page size, ECC size, MLC, SLC
- High-speed PHY interfaces will also need to support asynchronous operation
- Toggle and ONFi 2 interfaces are very different at the electrical level
- I/O's and programmability are very important





Thank you

- To learn more about Denali Software's related IP at ChipEstimate.com
- Use Denali IP to plan your next chip!
- Please stay and talk with Bob Pierce

