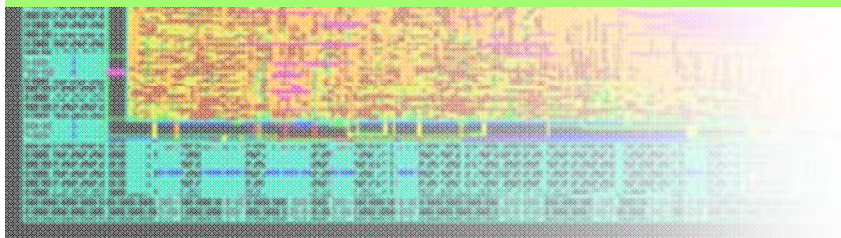


Richard F Zarr  
Technologist



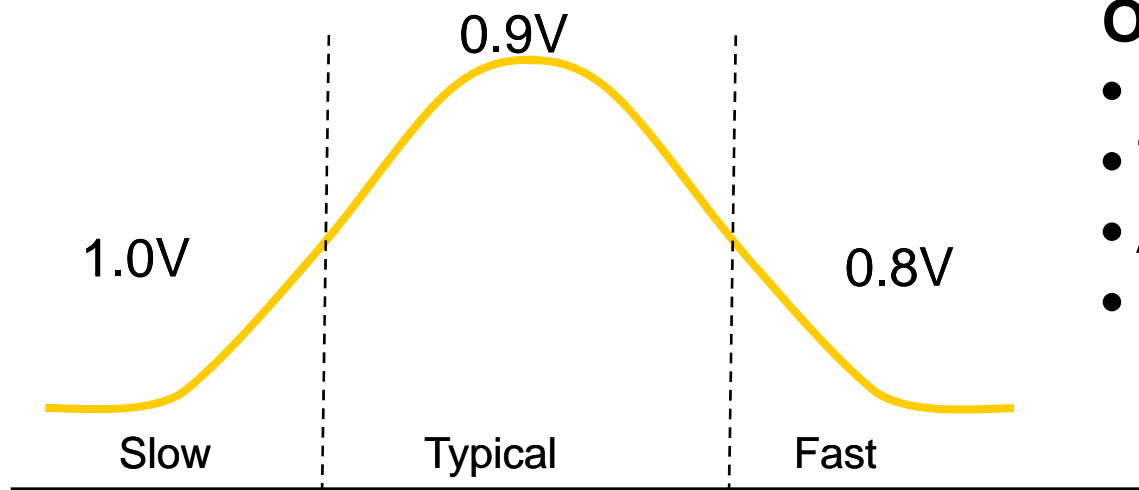
# CMOS Energy Fundamentals



- Basic CMOS power equation

–  $\text{Power} = \alpha C f_{\text{clock}} V^2 + V I_{\text{leakage}}$

- $\alpha$  ,  $C$  : Process dependent,  $V$  : Supply voltage,  $f$  : Frequency

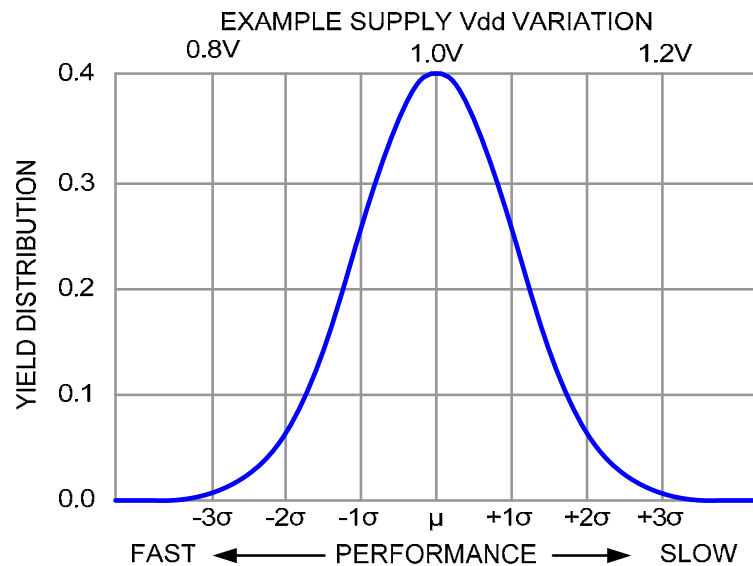


## Operating voltage depends on:

- Process variation
- Temperature variation
- Aging
- Frequency



# Example Statistical Power Savings



$$\frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} e^{-\frac{x^2}{2}} dx = 1 \quad \text{Normalized Gaussian distribution function}$$

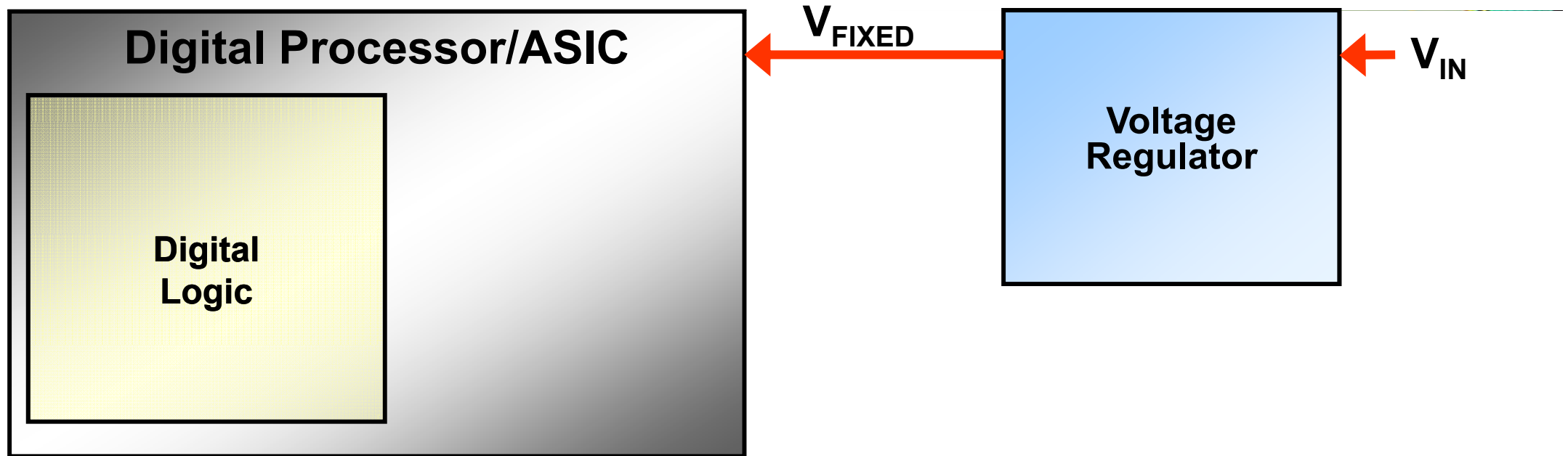
$$\%_{CMOS} = \frac{1}{\sqrt{2\pi}} \int e^{-\frac{x^2}{2}} \left( \frac{\frac{x}{15} + 1}{1.2} \right)^2 dx \quad \text{(Dynamic power only)}$$

$$\%_{CMOS} = 0.001233 \left( e^{-\frac{x^2}{2}} (-x - 30) + 283.249 \operatorname{erf} \left( \frac{x}{\sqrt{2}} \right) \right) \Bigg|_{-3}^{+3} = 0.696$$

With a variation of 0.8V to 1.2V over 99.7% of the yield adaptive methods can provide over 30% reduction in total power even ignoring static power savings.



# Traditional Power Management Delivery

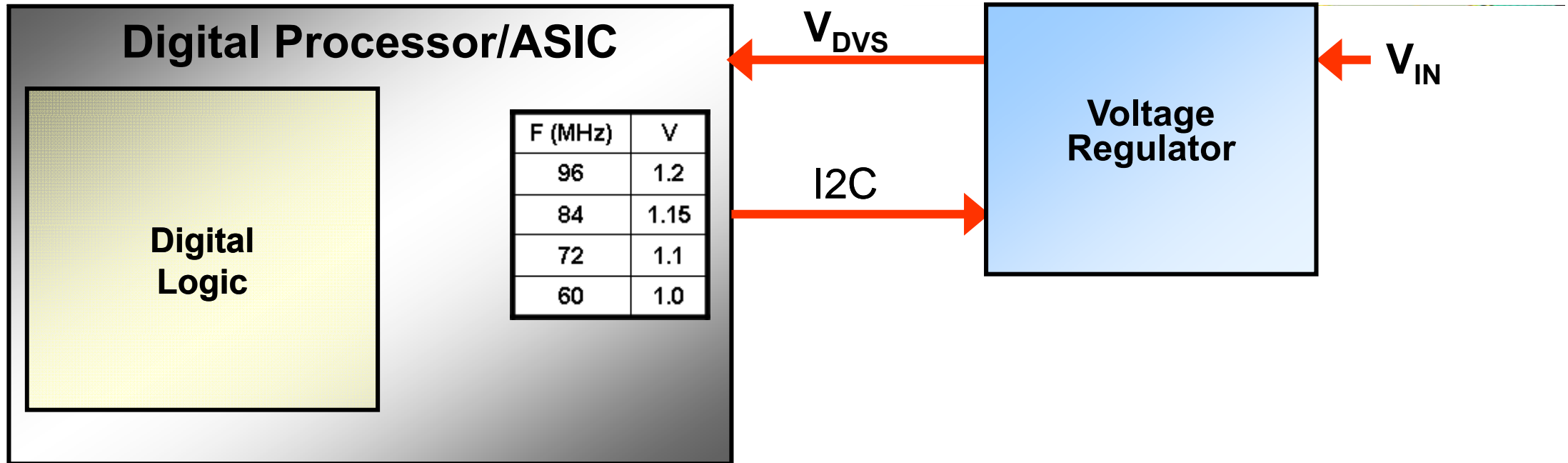


Inefficient system using fixed voltage

- No temperature compensation
- No adjustment for lower voltages at lower frequencies
- No compensating for process variation



# Dynamic Voltage Scaling (DVS)

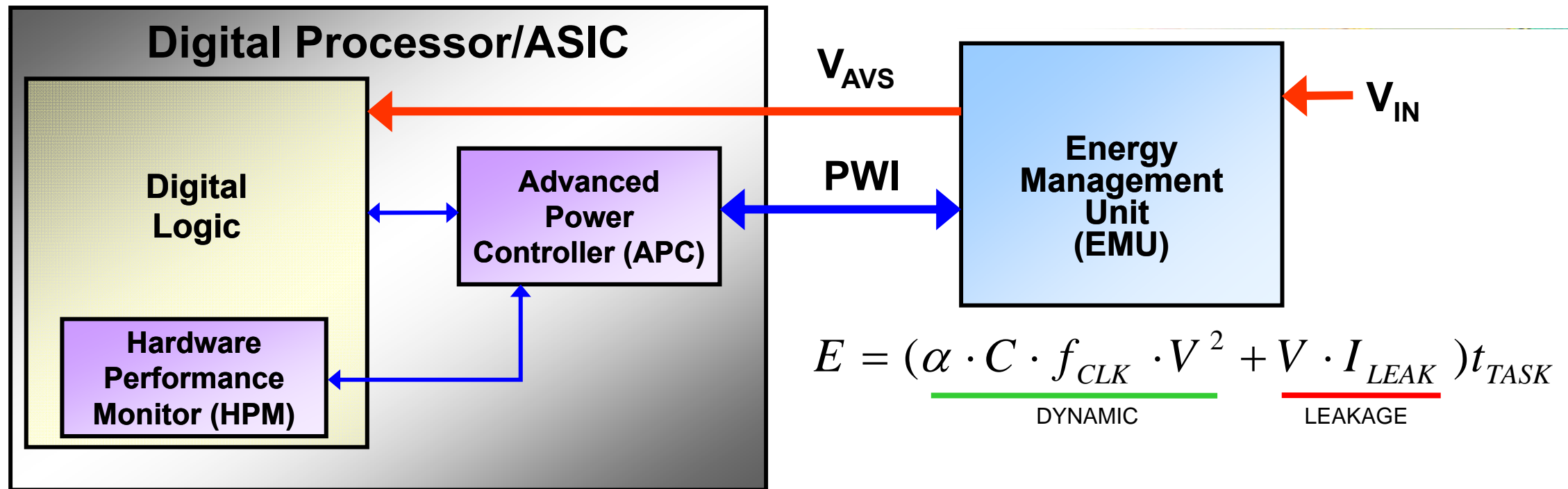


## Dynamic Voltage Scaling (Still inefficient)

- No temperature compensation
- No compensating for process variation
- No savings at max operating frequency



# PowerWise<sup>®</sup> Adaptive Voltage Scaling (AVS)



$$E = \underbrace{(\alpha \cdot C \cdot f_{CLK} \cdot V^2)}_{\text{DYNAMIC}} + \underbrace{V \cdot I_{LEAK}}_{\text{LEAKAGE}} t_{TASK}$$

Adaptive Voltage Scaling (Most efficient)

- Process and Temperature Compensation
- No need for frequency-voltage lookup tables
- Real-time continuous closed-up



PWI = PowerWise Interface

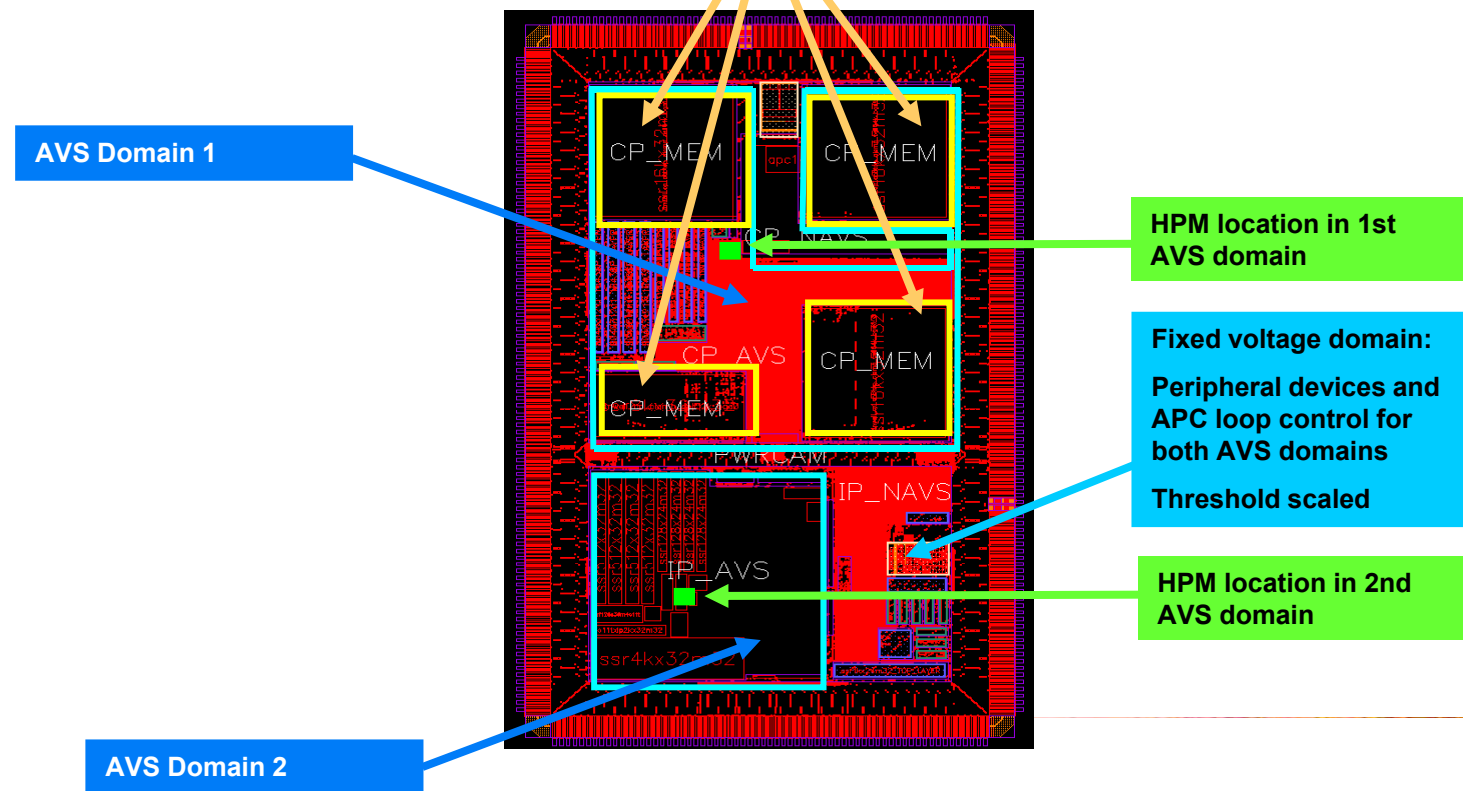


# Multiple AVS domain Example

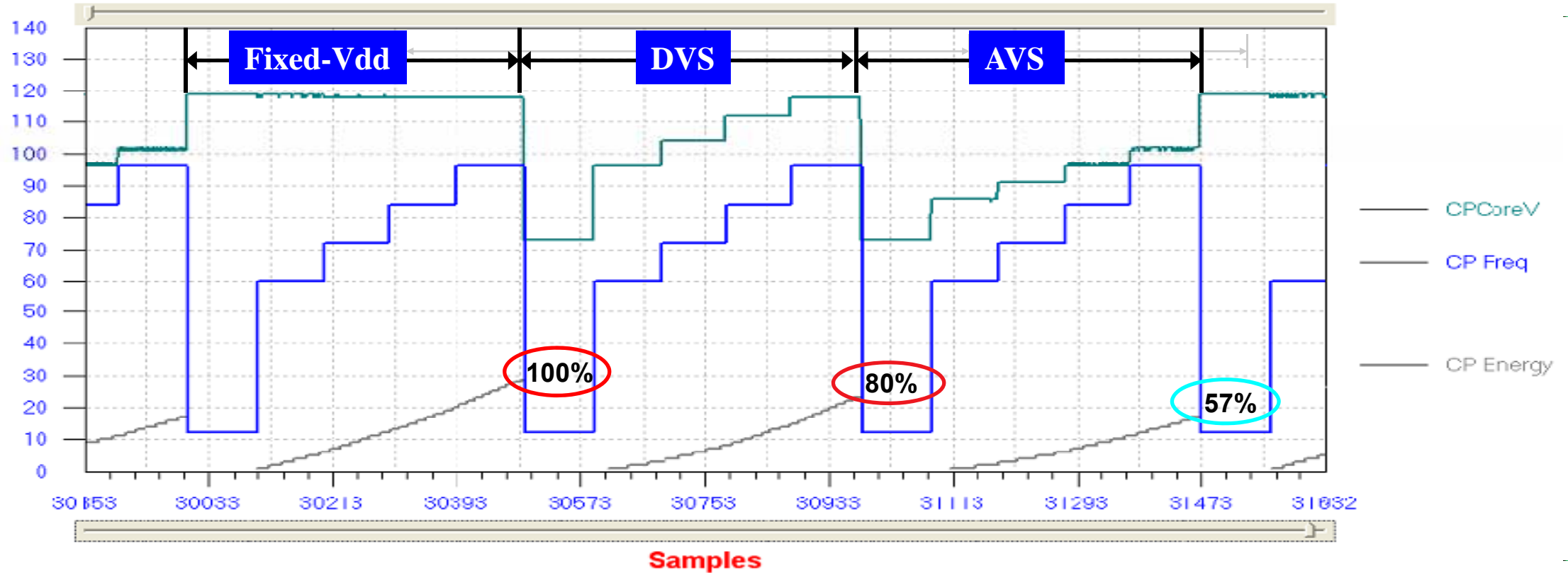


- Dual ARM7 CPU cores
  - 96MHz design
- Two AVS domains
  - Two ARM7 AHB clusters
  - APC in fixed Vdd domain
  - HPM in AVS(1)
    - Logic
  - HPM in AVS(2)
    - Logic
- Memory retention domains
- Fixed voltage domain
  - APB clusters

Memory Retention Domain (Memory voltage is maintained when AVS Domain 1 is off in retention mode)



# Dhrystone Benchmark Results



AVS enables 43% energy savings over fixed voltage



# Thank you



- Explore more about National Semiconductor Adaptive Voltage Scaling Technology and related IP at [ChipEstimate.com](http://ChipEstimate.com)
- Use IP specific to National Semiconductor to plan your next chip!
- Please stay and talk with Rick Zarr

