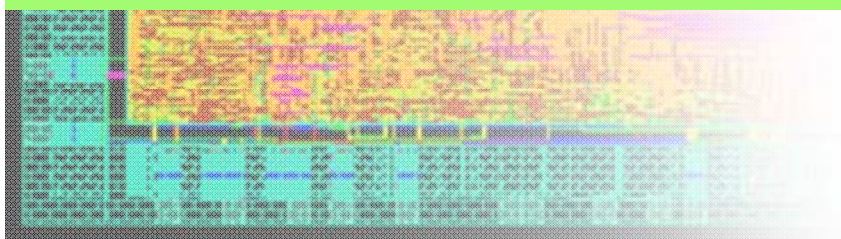


**Uniquify**

ASIC design & IP solutions

Customized DDR IP Solutions  
and IP Integration Services

Mahesh Gopalan  
Director, ASIC Engineering



**ChipEstimate.com**<sup>™</sup>

# Corporate Profile



- **Uniquify is a leading edge supplier of ASIC design and IP services focusing on complex multi-million gate System-on-Chip (SoC) designs supporting 40nm/65nm/90nm technology**
- **Extensive expertise in ASIC program management and execution**
- **Based in Silicon Valley targeting US customers**
- **Proven team of 55 physical and logical design experts**
- ***Perseus* ASIC Automation Flow enables great execution in complex SoC designs**
- **Effectively manage Project Risks by exposing challenges early**
- **Collaboratively working with our Clients' Design Teams to optimally resolve challenges**
- **Goal: meet or exceed schedule, financial, technical objectives**



## Why is DDR so tough? (Logic Design Challenges)

- **Challenges in integrating external IP into user's system**
  - Performance requirements / traffic patterns vary widely from system to system.
  - Memory controller IP may be optimized for a different kind of traffic pattern from what the user experiences in his system.
  - User Bus interface may not match IP vendor's bus interface.
- **Various sources and sinks of traffic**
  - Different agents need different share of bandwidth.
  - Latency versus performance goals. Conflicting cost functions.
  - Coherency requirements.
- **On chip data buffering**
  - Temporary storage for data that's on it's way to DRAM / coming back from DRAM on chip.
  - Needed for redistributing peaks and troughs in traffic
  - Needed to enable proper sharing of DRAM bandwidth.



# Uniquify's solution

- **Individual ports for every source of traffic**
  - Allows fine control over rate of data transfer and latency seen by each source.
  - Accurate sharing of total available bandwidth for maximum achievable performance.
  - 31 port design runs at 400MHz in 90nm node.
- **Dedicated buffers for each port**
  - Evens out peaks and troughs in traffic patterns for sustained throughput.
- **Optimize DDR bandwidth utilization**
  - Use DDR memory bank based architecture to hide access latency.
  - Combine writes together and reads together to hide write to read switching penalties.
- **Bus interfaces supported by Uniquify:**
  - AHB, AXI, Uniquify's custom FIFO based interface
- **Special bus interface features:**
  - Can handle data aligned to starting address or data aligned to byte 0.
  - Bus width converters to interface memory controller to any user bus width.
  - Reads and writes are processed independently on each port. They do not block each other because of FIFO full / empty conditions. (But data coherency is still checked!)



# Integration services

- **Logical integration services**
  - Customize how the controller fits in with the user's bus architecture.
- **Performance optimization services**
  - Customize arbitration considerations and parameters.
  - Create a custom tailored test environment to match user's application.
  - Provide feedback to user on bottlenecks in design and ways to increase performance.
  - Help user meet latency and throughput requirements.



## Why is DDR so tough? (Physical Design Challenges)

- **System level timing margin requirement is often not available**
  - There are many different types of DDR SDRAM memories
  - Package timing is not well characterized
  - Board trace delay numbers are not exact most of the times
  - IO delay numbers are not accurate due to wide range of loads
- **Physical implementation can be quite challenging**
  - Difficult to meet data/clock skew requirement across byte-lanes
  - Appropriate design constraints are hard to derive from system level timing spec
  - Floorplan can be a headache due to a long span of IO's
- **Integration of various DDR IP's from multiple vendors is not trivial**
  - Logic designers have to thoroughly understand DLL/PLL/SSTLIO capability and functionality
  - DDR controller design without physical implementation consideration can lead to a very long turn-around time



# Uniquify's **SCL** (Self Calibrating Logic)



- **Self calibrating Logic that solves system level timing issues.**
  - Auto-adjusts all read capture timings for DDR2 & DDR3.
  - Auto-adjusts write timing as well in the case of DDR3.
  - Solves all clock domain crossing issues.
  - Many cycles of skew between byte lanes can be compensated for by SCL!
- **SCL is run every time on power up.**
  - Can also be run on the fly with minimum performance overhead.
- **Guarantees the best possible operating timing margins.**
  - Calculates the passing window for each timing related parameter
  - Timing parameters are programmed in the middle of the passing window to ensure the best possible system-level timing margin
- **DRAM related failures are detected right away.**
  - Assures reliable in field operation.



# Uniquify's **SCL** (Self Calibrating Logic)

(Continued)



- **Works without user intervention.**
  - User is freed from having to learn about the complexities of meeting DDR2 / DDR3 timing.
  - Effortless and easy lab bring-up. User does not have to learn about phy registers and their programming options.
- **Ease of timing closure at high speed.**
  - No need to fuss over calculating exact round-trip timing
  - P&R team can just concentrate on internal flop-to-flop timing closure between controller and phy.
- **Increases chip/system yield at production.**
  - Reliable at speed DDR operation can be verified on the tester.
  - Connect external DRAM or run SCL in loopback mode.
- **Guarantees low read data capture latency.**
  - No need for FIFO in the PHY.
  - SCL guarantees theoretical low read data capture latency.
  - Fast turn-around time between read and write operations



## DFI PHY Overview

- DFI 2.0 Compliant
  - Operates in Phy independent mode.
- Highly configurable/flexible
  - Compiler is tuned for Industry standard library set.
  - Supports rectilinear shapes.
- Supports industry standard 3<sup>rd</sup> party DDR SSTL IO's
- Phy Chaining
  - SCL related signals are passed between data phys and control phy through direct phy edge to phy edge connections.
  - Core area not used for SCL related signalling
- Separate register interface to the control lane.
  - Eliminates signal routes from external register block to phy.



# Thank you

- Explore more about Uniquify Inc. and related IP at [ChipEstimate.com](http://ChipEstimate.com)
- Use IP specific to Uniquify Inc to plan your next chip!
- Please stay and talk with Mahesh.

