Inno-Logic
ASIC.FPGA.Embedded

Dinesh Tyagi
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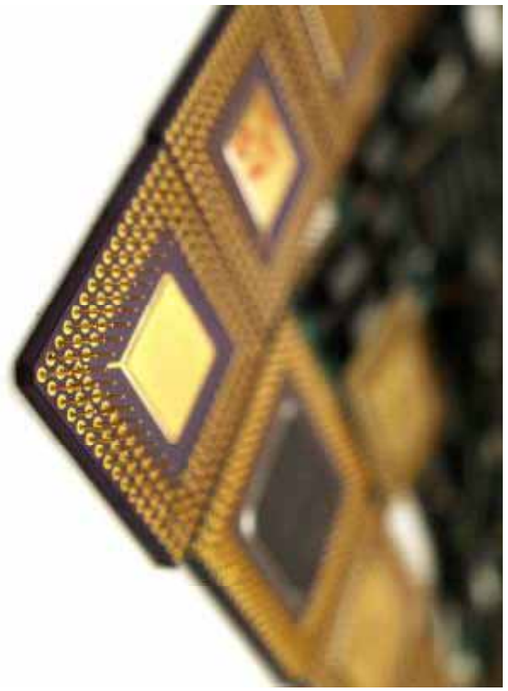

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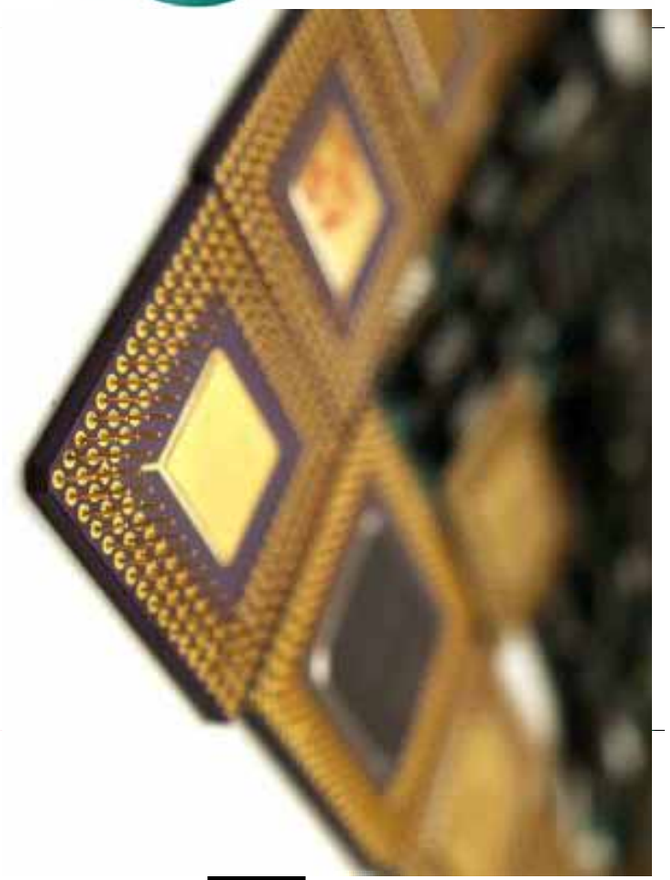
Innovative Logic

- Leading Provider of Design Services and Soft IP
  - Services
    - ASIC, FPGA, Embedded
  - Soft IP
    - USB3.0, UWB, WUSB
- Headquartered in Santa Clara, CA
  - With Design Center in Bangalore, India
- Some of our Customers
  - Intel, AMD, NEC, SanDisk, Renesas, Tivo, PLX
- Founded in April, 2005
    - Dinesh Tyagi



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Our Services and Our Soft IP

- Services
  - Logic Design Implementation
  - System Level Verification
  - Timing Closure and Timing Analysis
  - Design for Testability (DFT)
  - Physical Design and Verification
  - Silicon Validation & Board Bring Up
  - FPGA Design and Verification
  - Analog/Circuit Design & Verification
  - Embedded Systems Design

- Our Soft IPs
  - USB3.0 Device Controller
  - USB3.0 Host Controller*
  - UWB MAC Controller
  - Wireless USB Device Controller
  - AXI2AHB Interface
  - DMA Controller

*Available in Aug, 2009

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Key Features of our Soft IP

- Fully Synthesizable RTL code
- SystemVerilog based Verification environment
- User friendly RTL code with detailed comments
- Extensively verified with code coverage of at least 95%
- Cross verified with reputed 3rd party VIPs
- Dedicated Support:
  - In-Person, Phone, Email
- Developed by a team with Extensive experience in Soft IP
- Detailed Documentation including User Manual

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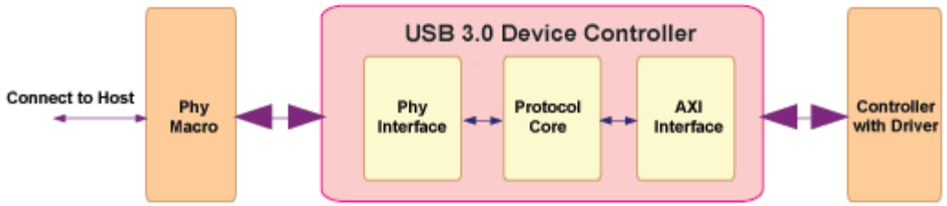
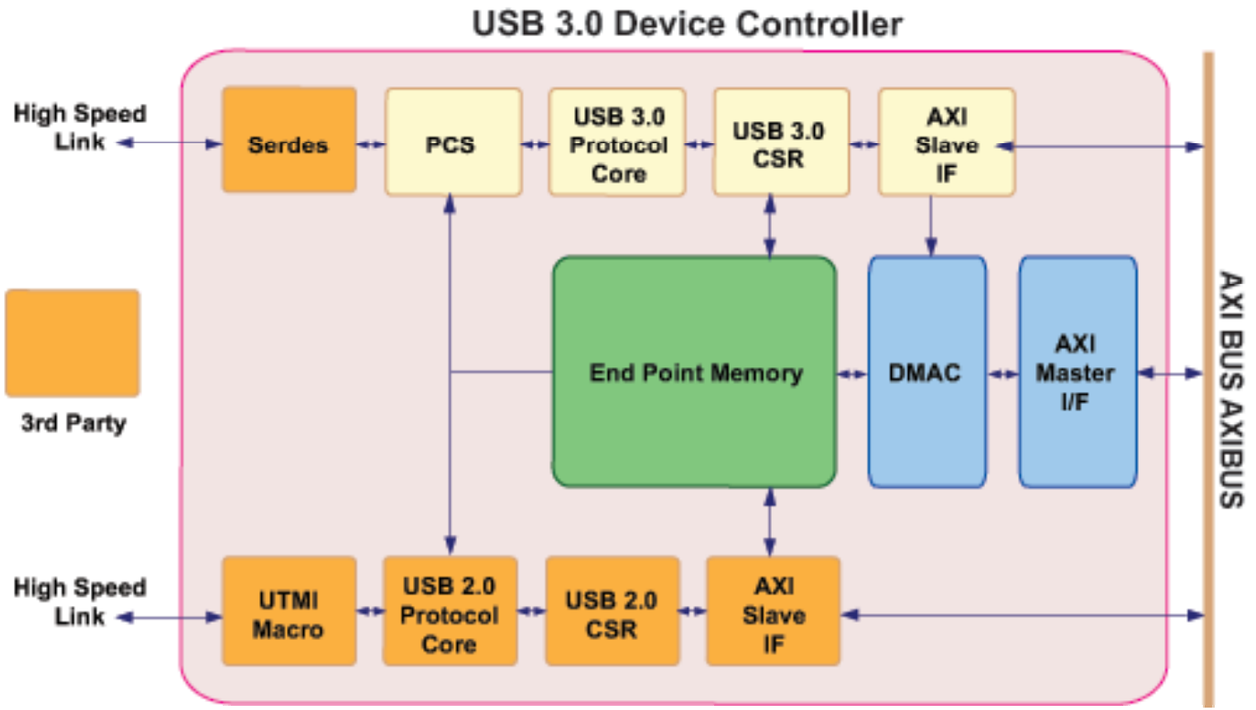
USB 3.0 Device Controller

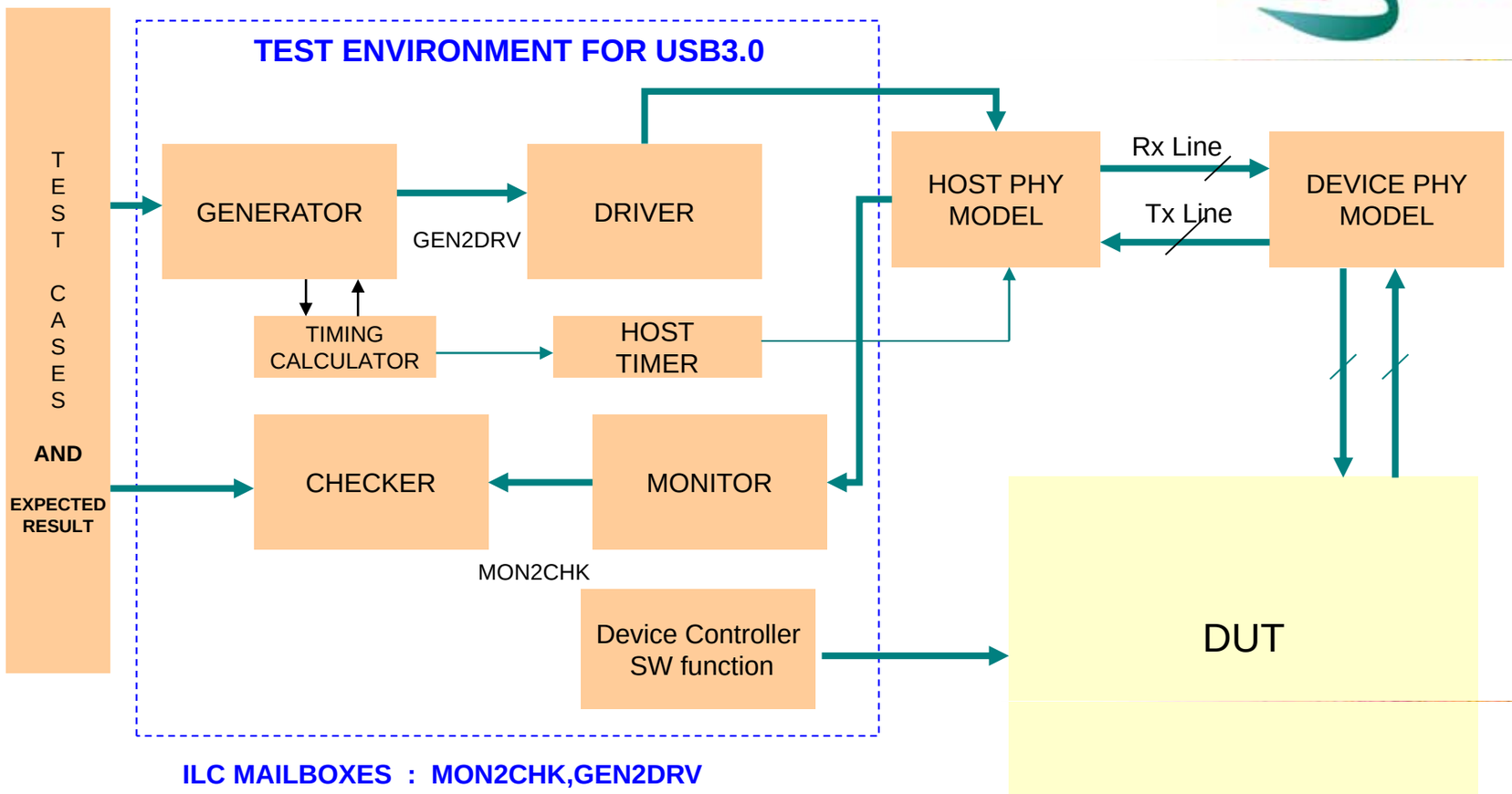
- Key Features
  - Fully compliant with USB 3.0 Spec 1.0
  - Fully Compliant with PIPE 3.0 Interface
  - Supports Industry Standard Interfaces – AXI, AHB
  - Support all transfer types
    - Control, Bulk, Isochronous and Interrupt transfers
  - Supports Bulk Streaming mode
  - Configurable up to 15 IN and 15 OUT endpoints
  - Contain 1 Control Endpoint
  - Endpoints are Configurable through software
  - Fully integrated DMA controller
  - Supports full Power Management
  - Fully integrated PIPE Compliant PCS Layer



Inside USB 3.0 Device Controller



USB 3.0 Verification Environment



USB3.0 PCS Layer

- Transmitter
  - Scrambler
  - 8B/10B Encoder
  - Skip Symbol Insertion State Machine
  - Support for Clock Dithering
  - Support for Generation Compliance pattern
  - LFPS Generation
- Receiver
  - Control Symbol Decoder
  - Equalization and Training Set Decoder
  - Calibration of the Receiver Serdes
  - 8B/10B Decoder
  - Elasticity Buffer
  - Skip Symbol Decode Logic
  - LFPS Decoding
  - Programmable Polarity of the Receiver Lane

Deliverables & Benefits

- Deliverables
  - Fully Synthesizable RMM Compliant RTL code
  - Complete SystemVerilog based Verification Environment
  - Scripts and Constraints File
  - User Manual, FAQ, etc.
- Benefits
  - Easy to migrate to any ASIC/FPGA Technology
  - Easy to integrate in current SOC Designs
  - Easy and Simple upgrade for current USB2.0 Customers
  - Easy to Configure for your Customized needs

Some of the USB 3.0 Applications

IP Talks!

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- Innovative Logic's USB3.0 IP
  - Highly Configurable, Synthesizable, Extensively Verified, Compliant to USB3.0 rev1.0
- Very Flexible Licensing Model based on your needs
  - Single Use, Unlimited Use, Source code, FPGA
- To Explore more about Innovative Logic's USB3.0
  - Visit ChipEstimate.com
- Innovative Logic's USB3.0 IP is ready to Integrate in your Design
- Any Questions
  - Please talk to Dinesh Tyagi, President & CEO
  - dtyagi@inno-logic.com

Thank you

- Explore more about **Innovative Logic** IP at ChipEstimate.com
- Use IP specific to **Innovative Logic** to plan your next chip!
- Please stay and talk with Dinesh Tyagi

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