



Using Customizable Processors in the SOC Dataplane

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Chief Scientist

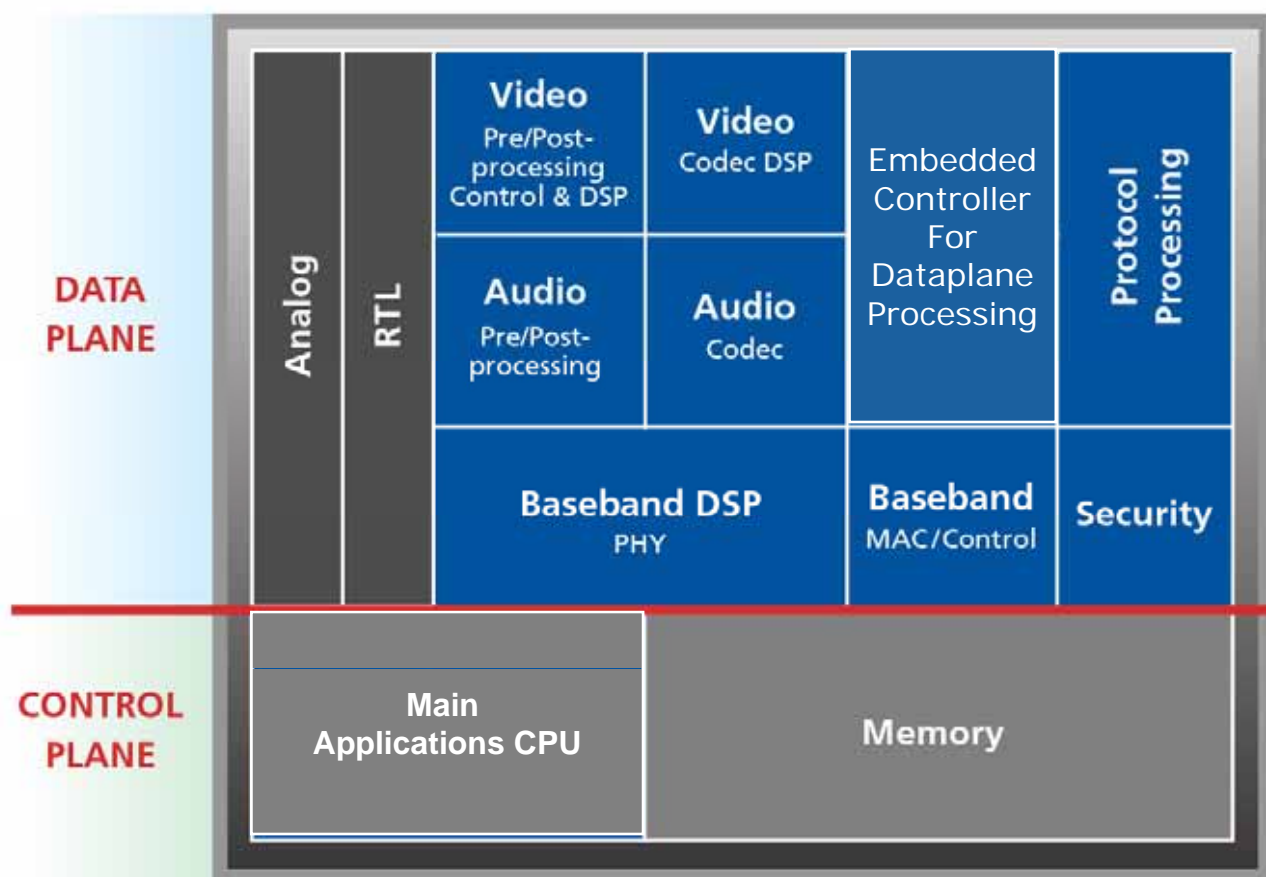
Fastest Growing Processor / DSP IP Company

- **Customizable Dataplane Processor/DSP IP Licensing**
 - Leading provider of automated, customizable Dataplane Processor Units (DPUs): a unique combination of processor & DSP IP cores + software design tools
 - Customization enables improved power, cost, performance
 - Standard DPU solutions for audio, video/imaging & baseband comms
 - Dominant patent portfolio for configurable processor technology
- **Broad-Based Success**
 - 140+ Licensees, including 5 of the top 10 semiconductor companies
 - Shipping in high volume today (>200M/yr rate)
 - **Fastest growing Semiconductor Processor IP company (Gartner):**
 - 21% revenue growth in 2007, 25% in 2008



Focus: Dataplane Processing Units (DPUs)

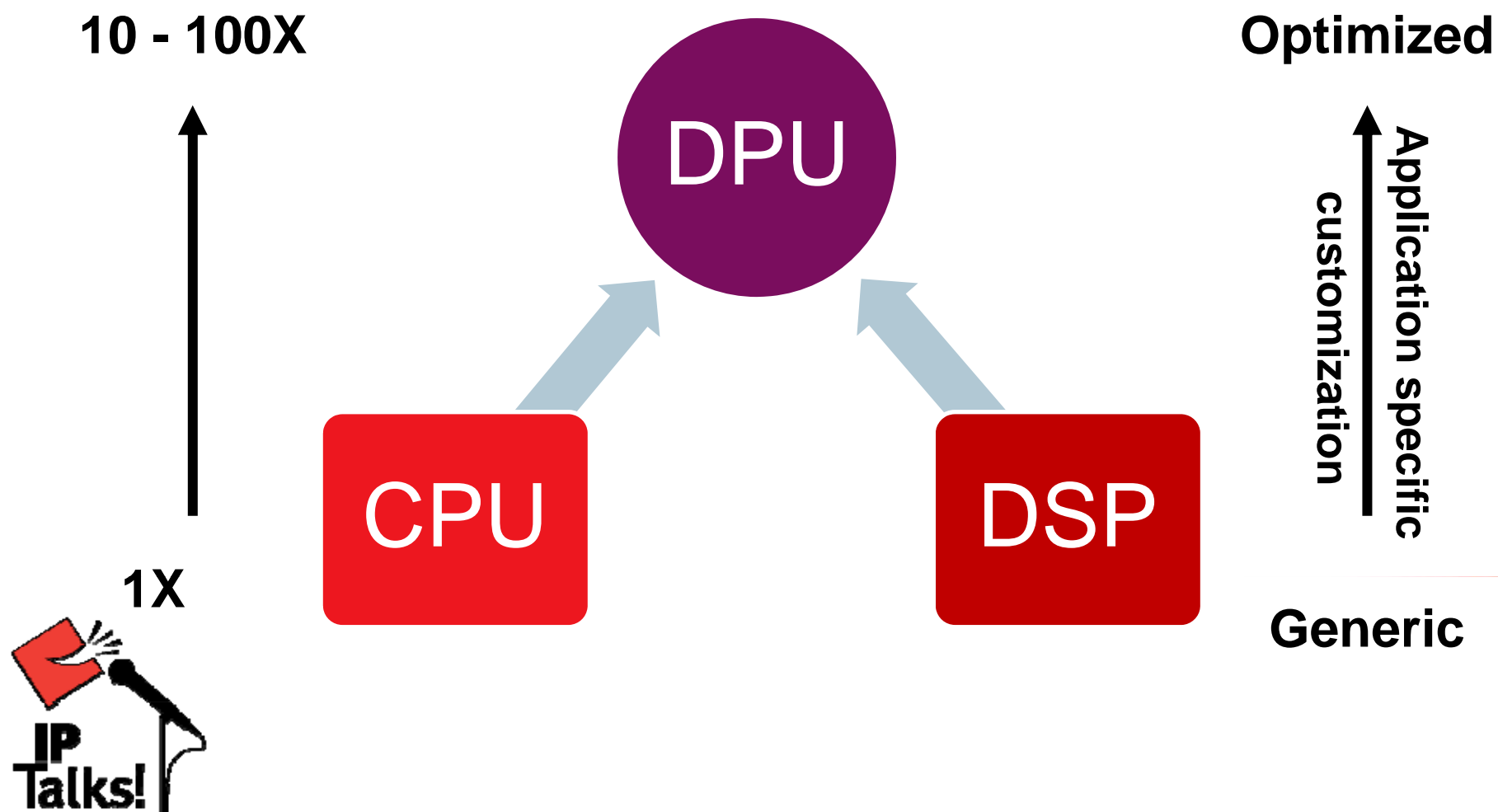
DPUs: Customizable CPU+DSP delivering 10 to 100x higher performance than CPU or DSP and providing better flexibility & verification than RTL



■ Tensilica fit and success – Embedded Control and DSP



DPU's Deliver Best of CPU and DSP at 10-100x Performance



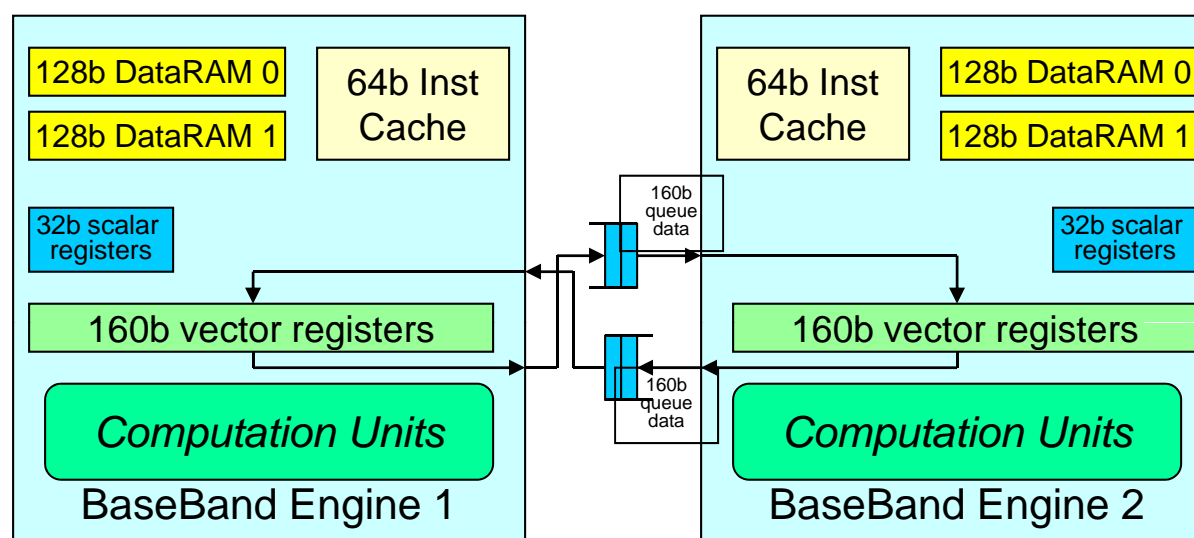
Dataplane Processors (DPUs)

- **Customization/optimization yields 10x to 100x performance over general purpose CPU/DSP**
- **Speed/power improvement from customized operation units & unique interfaces enabling fast In/Out dataflow**
 - Ports and Queues enable over 1,000 load, execute and store per cycle
- **Compared to fixed RTL, programmability enables performance tuning and bug fixes via firmware upgrade**
 - Lowers design risk and faster time to market
 - Increase market applications
- **Better verification infrastructure over RTL or in many cases over in-house programmable processor/DSP**
 - Processor-class verification tools

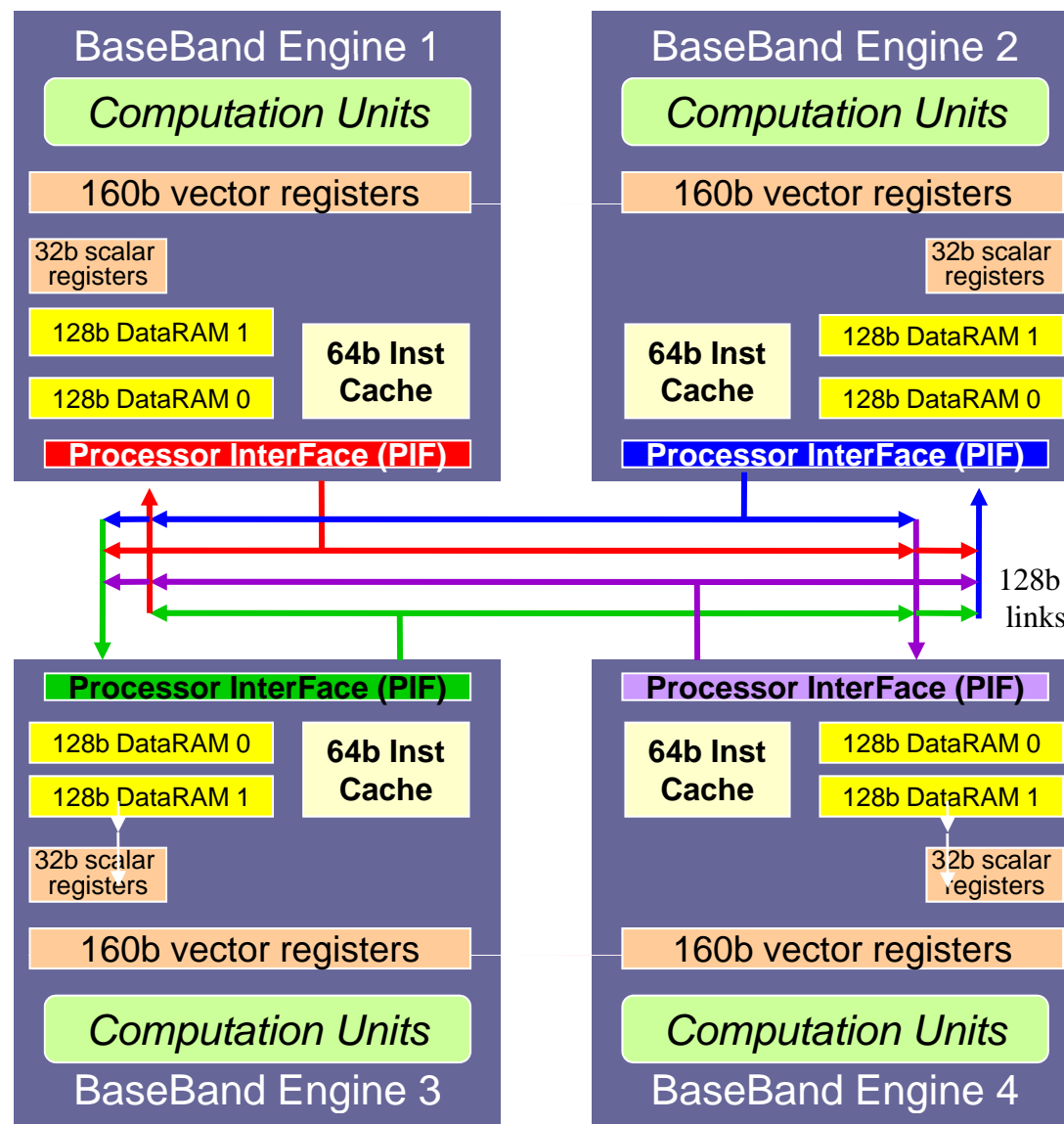


Fast I/O Let Tensilica Processors Bypass the Bus

- Example: Baseband processing
- 160b input and output queues implement hardware message passing at 8GB/s
- Full hardware handshake and software support to implement data sharing and synchronization among cores
- Much lower energy and higher bandwidth than bus-based data sharing



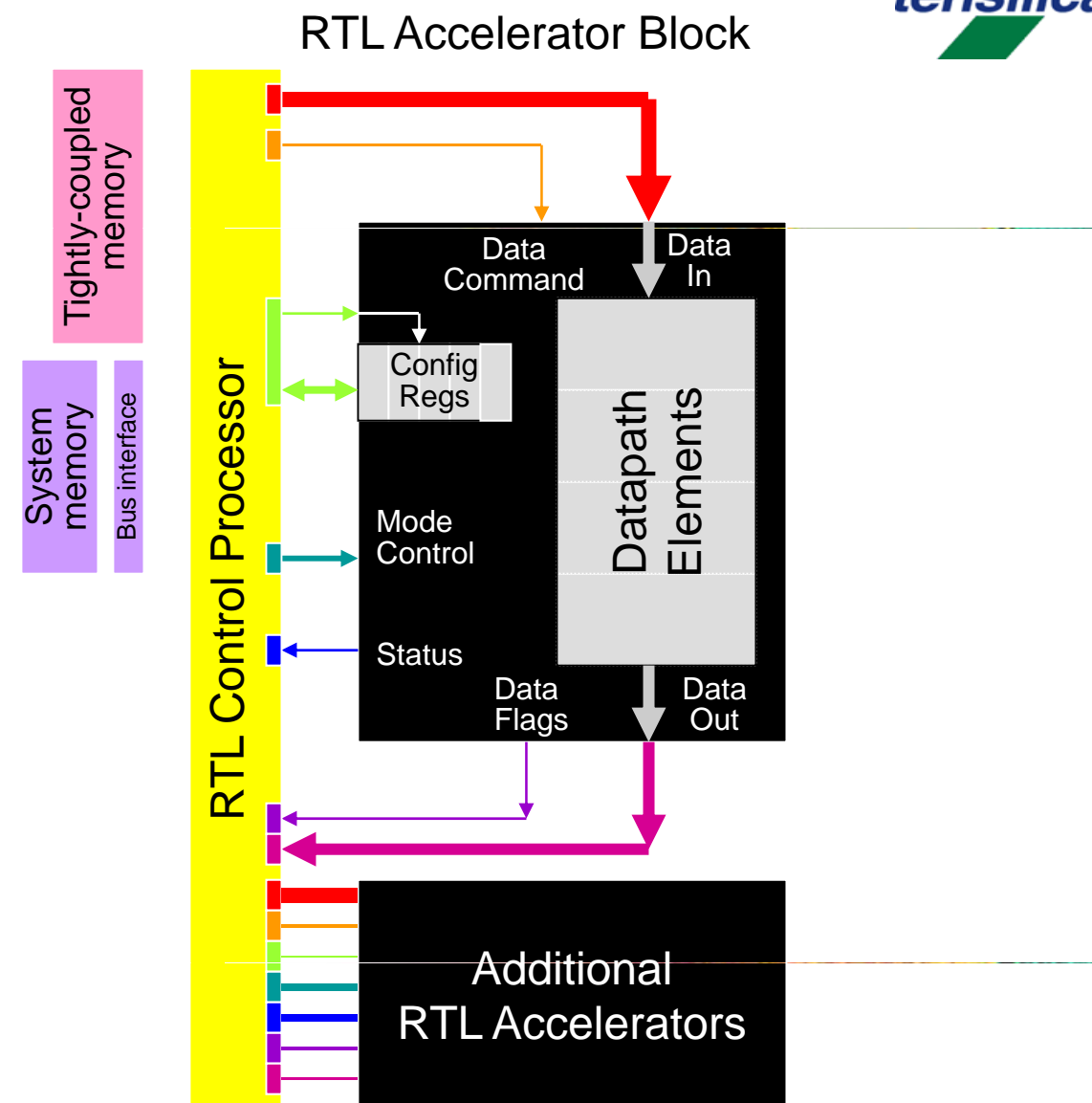
- 2-8 Baseband Engines form powerful shared memory baseband processor platform
- 8 engine cluster:
 - 128 MACs/cycle
 - Up to 640 ops/cycle
 - 880K 2048pt complex FFTs per second
- Distributed DataRAM space visible to all engines accessed across 128b pipelined interconnect
- Write-buffered interface allows aggregate 120GB/s processor load/store data bandwidth and 60GB/s inter-engine data bandwidth (at 500MHz)
- Native SystemC modeling of multi-engine processors, including cycle-accurate and fast “Turbo” mode bit-accurate simulation



Multiple RTL Blocks Controller by a Processor

- RTL Accelerator blocks have a wide variety of interface types and widths
 - Data input stream
 - Data output stream
 - Data command inputs
 - Data output flags
 - Configuration registers
 - Mode control
 - Status outputs
- Extensible processor matches RTL interface type and width (to 1024b)
 - Output queues
 - Input queues
 - Read only lookups
 - Read/write lookups
 - Import wires
 - Export states
- Full software support for interfaces:
 - Mapped to instructions and compiler
 - Modeling in high-level and RTL tools
 - Visible to source debugger

Processor performs “smart DMA” for RTL data transfers



Thank You

- Explore more about Tensilica and related IP at www.tensilica.com
- Use DPUs from Tensilica to plan your next chip!
- Please stay and talk with Grant Martin

